by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,799,179

Handling of exceptions in speculative instructions
Filed: January 24, 1995 Issued: August 25, 1998
Assignee: IBM Claims: 59
Inventors: Kemal Ebcioglu et al.
A method and system for handling speculative exceptions while parallel-processing sequential code is disclosed. In response to a speculative exception, the address of the instruction causing the exception is stored, along with an exception condition and at least one operand of the instruction. When a nonspeculative instruction requiring the operand is executed, the exception is reevaluated by reexecuting the instruction causing the speculative exception.

5,797,025

Processor architecture supporting speculative, out of order execution of instructions including multiple speculative branching
Filed: November 14, 1996 Issued: August 18, 1998
Assignee: Hyundai Claims: 17
Inventors: Valeri Popescu et al.
A processor architecture is described where instruction-fetching functions are decoupled from instruction-execution functions by a dynamic register file. Fetching operates in free-running mode, which does not stop if a fetched instruction cannot be executed due to data dependencies. Branch instructions are predicted and speculatively performed.

5,794,066

Apparatus and method for identifying the features and the origin of a computer microprocessor
Filed: May 7, 1995 Issued: August 11, 1998
Assignee: Intel Claims: 15
Inventors: Robert S. Dreyer et al.
A multilevel identification apparatus and method for providing at least a first type identifying the origin of a microprocessor and the number of levels of identification information available, and a second type for identifying a family, a model, a stepping ID, and features of a microprocessor. The microprocessor has first and second memory elements for storing the information.

5,794,029

Architectural support for execution control of prologue and eplogue periods of loops in a VLIW processor
Filed: October 18, 1996 Issued: August 11, 1998
Assignee: Elbrus International Claims: 19
Inventors: Boris A. Babaian et al.
For certain classes of software-pipelined loops, prologue and epilogue control is provided by loop-control structures rather than by predicated-execution features of a VLIW architecture. Loop-control logic includes loop-control registers having an epilogue-counter field, a shift register, a side-effects-enabled flag, a current-loop-counter field, a loop-mode flag, a side-effects manual-control flag, and a load manual-control flag.

5,794,027

Method and apparatus for managing the execution of instructons with proximate successive branches in a cache-based data processing system
Filed: February 21, 1997 Issued: August 11, 1998
Assignee: IBM Claims: 15
Inventors: Gregory Grohoski et al.
A small buffer called a branch-anticipate buffer (BAB) is used to store groups of instructions that are likely to be required from the instruction cache (I-cache) when an instruction prefetch miss occurs. When a prefetch miss occurs, the BAB is checked to see whether instructions corresponding to the target address are available. If they are available, they are copied into an appropriate buffer. If they are not, these instructions are fetched from the I-cache and placed into a buffer and, selectively, into the BAB. The BAB maintains only branch-target addresses that have not been previously scanned and that cannot be prefetched in time.

5,781,752

Table based data speculation circuit for parallel processing computer
Filed: December 26, 1996 Issued: July 14, 1998
Assignee: Wisconsin Alumni Research Claims: 9
Inventors: Andreas I. Moshovos et al.
A data-speculation circuit for an out-of-order processor is disclosed. Data-consuming instructions may be speculatively executed before their data-producing counterpart instructions are executed. Thresholds for misspeculations associated with speculative data-consuming instructions may be established, allowing stoppage of speculative execution of the particular data-consuming instruction that exceeds the threshold specified.

OTHER ISSUED PATENTS

5,799,165 *Out-of-order processing that removes an issued operation from an execution pipeline upon determining that the operation would cause a lengthy pipeline delay*
5,796,975 *Operand dependency tracking system and method for a processor that executes instructions out of order*
5,796,971 *Method for generating prefetch instruction with a field specifying type of information and location for it such as an instruction cache or data cache* M