Intel to Develop Network Processors

Intel has announced it will develop a new line of chips it dubs network processors. Described as "software-programmable forwarding and control engines," the chips are intended as replacements for hardwired ASICs in network switches, routers, and other infrastructure equipment.

Intel provided no details on the internal architecture or design of these new chips, and many have speculated that they might be nothing more than the deathless i960 family with different integrated peripherals and a new name. We believe, however, that the network processors will be significantly new chips, possibly with a new instruction-set architecture. Intel recently agreed to acquire Level One *(www.level1.com)*, a maker of networking equipment, and has completely absorbed Digital Semiconductor; between the two, Intel should have access to a number of interesting technologies.

More details will have to wait until later this year, when Intel will announce specifics of the chips. In the meantime, makers of switching equipment and suppliers of network silicon are wondering what cards Intel is holding. —*J.T.*

QED Cottons to Copper

At last week's Embedded Processor Forum, the denizens of QED, continuing a tradition of eminently practical if not profoundly ambitious CPU designs, rolled out their latest model for 2000. The RM7010 is an updated 64-bit MIPS core targeted for IBM's 0.18-micron copper process.QED *(www.qedinc.com)* expects first silicon of the RM7010 in early 2000, which could make it the first embedded processor to use copper.

At the microarchitectural level, the RM7010 changes almost not at all from the RM7000 (see MPR 10/28/96, p. 6). It has the same dual-issue pipeline with no branch prediction, but it halves the on-chip L2 cache to 128K. The cache excision was made because QED expects to use the RM7010 core in a range of highly integrated processors, not necessarily as a standalone CPU.

This strategy makes perfect sense; the RM7000 already addresses such market as exists for high-end 64-bit superscalar MIPS parts. Another standalone version with half the cache would be insufficiently differentiated to be worthwhile. On the other hand, the company's Alpine internal I/O structure (see MPR 12/28/98, p. 13) would make an ideal repository for an RM7010 brain. A high-end "Alpine II" product line with integrated PCI, network channels, and perhaps coprocessors, would make a fine basis for set-top boxes, fast printers, and networking equipment.

Although the prospect of 0.18-micron copper processing is exciting, the RM7010's expected frequency is less so. During his presentation, QED president and CEO Tom Riordan said he expects his latest brainchild to run at about 350 MHz—slow compared with the next-generation StrongArm (see MPR 5/10/99, p. 1), despite using copper processing. Part of the answer lies in the details of the CMOS-7SF version of IBM's process, which QED is using. Although it is denser than the preeminent CMOS-7S (see MPR 9/14/98, p. 1), its transistors are not as fast.

Nevertheless, it appears QED's devotion to a simple five-stage pipeline may be catching up with it. If the RM7010 can eke out only 350 MHz using one of the world's best fabrication technologies, it may be time for QED to get out its heavy pipefitting tools and do some serious plumbing. —*J.T.*

Lexra Debuts Radiax DSP Extensions for MIPS

At the Embedded Processor Forum, Lexra rolled out the latest version of its (mostly) MIPS-compatible core, the LX5280. Even more interesting, the company unveiled Radiax, Lexra's own set of DSP extensions for the MIPS architecture. In an unusual (and somewhat ironic) move, Lexra will license Radiax free of charge to any legal MIPS licensee.

The LX5280 enlarges Lexra's two-horse stable with a faster 200-MHz clock rate, a seven-stage pipeline, prioritized interrupts, and the promise of a soft (synthesizable Verilog) version of the core. At the Forum, Vice President and CTO Patrick Hayes said the new core will be available at the end of this year or early in 2000.

Many of the changes pace those made by Lexra's competitors. Intel's next-generation StrongArm (see MPR 5/10/99, p. 1) also lengthens its pipeline from five stage to seven, and PowerPC's Book E (see MPR 5/10/99, p. 9) adds two-level interrupts.

The bigger news was the introduction of Radiax, a set of 36 new DSP instructions and related enhancements to the LX5280's internal architecture. Radiax adds a second execution unit in parallel to the usual MIPS-I ALU and doubles up on the core's internal instruction and data buses. Both ALUs execute MIPS and Radiax instructions, although only one of the ALUs executes Radiax MAC operations.

The arrangement is more similar to Hitachi's SH-DSP than to ARM's Piccolo, in that the Radiax instructions are integrated with the MIPS instruction stream. There are Radiax instructions to, for example, load and store operands to and from memory. The 36 new opcodes include the usual 16×16-bit multiply and MAC operations. Radiax also adds saturating and fractional formats, and circular and post-adjusted addressing modes.

By giving it away, Lexra doubtless hopes to build support for Radiax among MIPS licensees, which could include Radiax extensions as long as they pass Lexra's compatibility test. Broad support would avoid Balkanization of the kind Intel's competitors narrowly avoided last year with disparate 3D extensions. It's ironic that Lexra should be licensing technology to MIPS vendors, since Lexra itself does not have a MIPS license. If Radiax is successful and broadly adopted, it will be sweet retribution for the company's lawyers. —*J.T.* M