by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,805,918

Dual-instruction-set CPU having shared register for storing data before switching to the alternate instruction set
Filed: October 24, 1995 Issued: September 8, 1998
Assignee: S3 (from Exponential) Claims: 9
Inventors: James Blomgren et al.
A dual-instruction-set CPU is capable of executing RISC instructions and CISC instructions. The registers in the CISC instruction set are merged or folded into some of the registers in the RISC architecture, so that these merged registers are shared. The flags registers and the general-purpose registers are merged, allowing a CISC program to pass data to a RISC program merely by writing one of its registers and switching control to the RISC program. The RISC program reads one of its registers, which is merged with and corresponds to the CISC register that was written to by the CISC program.

5,805,895

Method and apparatus for code translation optimization
Filed: June 9, 1996 Issued: September 8, 1998
Assignee: Motorola Claims: 17
Inventors: Mauricio Breternitz Jr. et al.
A native microprocessor accesses a block of foreign object code. An initial block scope defining translation parameters is assigned to the block. The block of foreign code is then translated to native code. An optimization efficiency is calculated for the translated block. A rescheduling criterion is established, based on the optimization efficiency. The block of native code is then executed. On subsequent accesses of the block, when the reschedule criterion is met, the block scope is redefined.

5,805,853

Superscalar microprocessor including flag operand renaming and forwarding apparatus
Filed: February 10, 1997 Issued: September 8, 1998
Assignee: AMD Claims: 3
Inventors: Scott White et al.
A superscalar microprocessor with a reorder buffer for storing speculative state and a register file for storing the real state of the microprocessor. A flags register stores the real state of flags. To enhance conditional-branch performance, the reorder buffer includes a flag-storage area for storing renamed flags that are updated by flag-modifying instructions. The microprocessor includes special buses for supplying the renamed flags to the branch unit.

5,805,850

Very long instruction word (VLIW) computer having efficient instruction code format
Filed: January 30, 1997 Issued: September 8, 1998
Assignee: IBM Claims: 15
Inventor: David Luick
Instructions in a VLIW CPU architecture consist of multiple parcels. Each parcel may contain an opcode, source and destination registers, special registers, immediate data, storage addresses, etc. The operations of at least some of the parcels are implied by the position of the parcel within the instruction word. A variable number of conditional branches, with a single destination target, may be specified by using some of the parcels, which would otherwise be used to specify operations in the ALUs.

5,802,337

Method and apparatus for executing load instructions speculatively
Filed: July 9, 1997 Issued: September 1, 1998
Assignee: Intel Claims: 14
Inventor: Kent Fielden
A load may be executed speculatively as a dismissible load instruction that does not take exceptions. A check instruction, in the same format as the dismissible load instruction, is then executed to determine whether an exception should be taken. In this manner, a load may be executed speculatively while ensuring that an exception occurs at the same time it would have occurred had the load been executed nonspeculatively.

5,802,336

Microprocessor capable of unpacking packed data
Filed: January 27, 1997 Issued: September 1, 1998
Assignee: Intel Claims: 11
Inventors: Alexander Peleg et al.
A processor that decodes an "unpack" instruction. The unpack instruction operates on two packed-data items. It produces a third packed-data item, which consists of fewer than all of the elements of the first packed-data item and corresponding elements of the second packed-data item.

OTHER ISSUED PATENTS

5,809,327 *Eight-bit microcontroller having a RISC architecture*
5,805,878 *Method and apparatus for generating branch predictions for multiple branch instructions indexed by a single instruction pointer*
5,805,876 *Method and system for reducing average branch resolution time and effective misprediction penalty in a processor*
5,802,338 *Method of self-parallelizing and self-parallelizing multiprocessor using the method* M