Nintendo to Battle PlayStation With PowerPC

Breathing new life into PowerPC, IBM and Nintendo have announced a multiyear billion-dollar deal for IBM to supply PowerPC processors to Nintendo for its next-generation game console, code-named Dolphin. The new DVD-based console is scheduled for delivery before next year's holiday season—just in time to go head-to-head with Sony's PlayStation 2000. Nintendo also announced an agreement with home-appliance giant Matsushita (Panasonic) to put Dolphin in a variety of home-entertainment and networking equipment.

Neither IBM nor Nintendo released any technical information on their new PowerPC processor, code-named Gekko. As a result, it is impossible to tell how the part will stack up against Sony's Emotion Engine (see MPR 4/19/99, p. 1). IBM and Nintendo, however, both expressed confidence that Gekko will have 3D-graphics game performance second to none. IBM said that the chip will be heavily customized for Nintendo, operate at 400 MHz, and be built in IBM's 0.18-micron copper CMOS-8 process in its Burlington fabs. Although 400 MHz is well below the capability of CMOS-8, IBM is undoubtedly being conservative to assure maximum yield and lowest cost.

Indeed, Gekko will have to be heavily customized, as no existing or planned scalar PowerPC core comes close to matching the floating-point power of the Emotion Engine. Although IBM refused to disclose the nature of the custom circuits on Gekko, the company does have access to the AltiVec SIMD-FP technology (see MPR 5/11/98, p. 1), which with dual units could supply the needed horsepower.

Gekko will be paired with a separate graphics chip, presumably in a functional partitioning similar to that between Sony's Emotion Engine and Graphics Synthesizer. Nintendo confirmed that Gekko's companion graphics chip, which will operate at 200 MHz, was designed by 3D-graphics company ArtX *(www.artxinc.com)* and will be manufactured by NEC using its embedded-DRAM/logic technology. Although Dolphin will have a system-memory bandwidth of 3.2 GB/s (just like the PlayStation 2000), Nintendo refused to disclose whether the platform would use DRDRAMs.

The IBM-Nintendo deal is a huge blow to MIPS, which had the inside track as the incumbent CPU in the Nintendo 64. Had MIPS landed Dolphin, it would have been at the heart of both of the leading game consoles; as it stands, MIPS must hope that Sony wins the console battle.

Although Sony seems the odds-on favorite, due to its market-leading position and the awesome capabilities of its Emotion Engine, the battle is far from over. Considering the difficulty of manufacturing the large Emotion Engine and Graphics Synthesizer chips and the complexity of programming the Emotion Engine's vector units, Sony could easily stub its toe. Also, Nintendo seems more clearly focused on the game-console function, and it is intent on shipping Dolphin at under $200 from the get-go—a price point that Sony may take some time to achieve. With IBM's semiconductor-technology prowess behind Nintendo, it's now Sony's turn to squirm. —*K.D.*

TI's 'C5000 Goes Low Power

At the recent Embedded Processor Forum, Texas Instruments, the market leader in programmable DSPs, announced low-power versions of its fixed-point TMSC5409 and 'C5402 DSPs. The 'C5409 is a new device targeting personal-audio applications and comes in three flavors: 100, 80, and 30 MIPS. The 'C5409 is pin compatible with TI's popular TMS320C549 and matches its 100 MIPS and 32K words of SRAM while adding new peripherals for more flexibility and improved system performance. The 'C5409 also has 16K words of ROM, three multichannel buffered serial ports (McBSPs), a six-channel DMA, an 8/16-bit host processor interface (HPI), and one timer. These devices are priced at $12.75 for the 100-MIPS version, $15.00 for the 80-MIPS version, and $16.50 for the 30-MIPS version in 10,000 unit quantities. The low-performance versions are more expensive than the high-performance versions, due to their lower power ratings.

The 'C5402, initially announced in September 1998, targets communication-centric client devices, such as wireless modems and IP-phones. It has 16K words of SRAM, 4K words of ROM, two McBSPs, a six-channel DMA, an 8-bit HPI, and two timers. The device comes in 1.8-V and 1.2-V versions, both of which are manufactured in a 0.18-micron process that gives them power/performance ratings of 0.72 and 0.36 mW/million MACs, respectively. Performance of these devices is 100 MIPS at 1.8 V and 30 MIPS at 1.2 V. The 80-MIPS and 30-MIPS versions of both the 'C5409 and 'C5402 have an option for variable I/O voltages. 'C5402s are priced at $5.40 for the 100-MIPS version, $6.50 for the 80-MIPS version, and $7.00 for the 30-MIPS version.

The DSP core in all of these devices is code compatible with the C5000 family. The core architecture of the C5000 family has remained the same since its inception, and TI has been primarily riding the process curve to improve performance and reduce power dissipation. TI has also used some clever circuit-design techniques and careful clock distribution strategies to further reduce power dissipation.

TI has also announced plans to build even lower power devices that will run at 1.5 V and at 0.9 V in a 0.15-micron process. These devices are expected to have power dissipations of 0.42 and 0.20 mW/million MACs, respectively. Some of the target applications for all these new devices are low-power telecom, blood-glucose monitors, heart-rate monitors, hearing aids, cochlear implants, solid-state voice recorders, MP3 audio devices, and noise-cancellation headphones. —*Krishna Yarlagadda* M