Intel Expands Embedded x86 Lineup

Narrowing the performance gap between desktop and embedded processors, Intel has introduced faster versions of Pentium II for lower-powered applications.

"Lower-powered," in this context, means about 9–13 W, depending on the clock frequency, the amount of L2 cache, and the level of integration. That's decidedly on the higher end of the embedded power envelope. But Intel points out that even line-powered appliances, such as set-top boxes, will find these versions of the Pentium II more useful than regular versions of the chips, because consumer appliances often have sealed cases with poor airflow.

Intel announced two Pentium II chips in surface-mount BGA packages and a pair of Pentium II embedded modules. All are variations of products Intel currently ships for mobile PCs. The BGA chips are Dixons clocked at 266 and 333 MHz with a 66-MHz system bus. Each has 256K of on-chip L2 cache, coupled to the CPU core over a full-speed backside bus. The BGA package measures $31 \times 35 \times 2.4$ mm. Typical power consumption is 8.8 W at 266 MHz and 11.8 W at 333 MHz. They're available now: 1,000-unit prices are $187 for 266 MHz and $316 for 333 MHz.

The Pentium II modules contain the CPU, the north bridge of a 440BX chip set, and a voltage regulator. The 266-MHz Deschutes version puts 512K of L2 cache in SRAMs on the module, coupled to the CPU over a half-speed backside bus. The 333-MHz Dixon version integrates 256K of L2 cache on-chip, with a full-speed backside bus. Both have a 66-MHz system bus. The module measures $2.5 \times 4 \times 0.39$ inches; typical power consumption is about 12.4 W with AGP disabled, or 13.4 W otherwise. They're available now; 1,000-unit prices are $246 for 266 MHz and $374 for 333 MHz.

By rapidly pushing PC-caliber processors into its embedded lineup, Intel is moving beyond the old attitude that the embedded market is a recycling bin for obsolete PC chips. Intel is also aiming at new-breed information appliances that don't fit the mold of traditional embedded systems. But along with that PC-caliber power comes PC-level prices and laptop-level power consumption. Most embedded designers will continue to look at other options, including Intel's own StrongArm chips. —*T.R.H.*

Motorola Enhances PowerPC Line

At last month's Embedded Processor Forum, Motorola announced a pair of PowerPC chips that make several improvements to the existing PowerPC 740 and 750 (see MPR 2/17/97, p. 10). The new 745 is a drop-in replacement for the 740, and the new 755 is compatible with the 750. Improvements include lower power consumption, lockable caches, and better support for memory management.

The two processors are nearly identical, except the 755 runs at higher core frequencies and has a backside bus for an L2 cache. Both are three-way superscalar machines with 32K instruction and data caches, a double-precision FPU, on-chip debug, and various low-power modes. Motorola will offer the 745 at frequencies of 300–350 MHz, while the 755 will be available at frequencies of 300–450 MHz.

Both chips will consume about 25% less power than their predecessors, thanks to a process shrink to 0.22 micron. Typical power consumption is estimated at 4.5 W or less at 400 MHz with a 1.9-V core. The I/O voltage is selectable between 1.8 V and 3.3 V. Packaging hasn't changed—a 255-pin BGA for the 745 and a 360-pin BGA for the 755—but Motorola plans to offer a PBGA in the future.

Programmers can lock the L1 instruction and data caches entirely or in 1–6 segments (4K per segment). Similarly, a program can configure the entire L2 cache as direct-mapped memory or split it 50/50 as cache and memory. These options allow critical algorithms (such as network routing lookups) and static data (such as tables) to stay resident in fast SRAM that's immune from cache transiency.

To further improve memory management, Motorola has doubled the number of block-address translation (BAT) registers for instructions and data—there are now eight registers for each. Motorola also added the option of software tablewalks; previously this was done only in hardware.

Motorola says it will announce availability of the 745 and 755 in 3Q99. Until Motorola announces processors that implement the new Book E embedded architecture (see MPR 5/10/99, p. 9), it makes sense to tweak the existing product line to keep it competitive. —*T.R.H*

Sun Offers Embedded UltraSparc IIe

Sun Microsystems announced a derivative of its UltraSparc II processor for embedded applications at last month's Embedded Processor Forum. The new UltraSparc-IIe will combine the 64-bit UltraSparc-2 core (see MPR 11/13/95, p. 20) with 256K of on-chip L2 cache, an integrated DRAM controller, enhanced power-management features, and a 32-bit 66-MHz PCI host bridge.

Built in Texas Instruments' 0.18-micron, six-layer-metal process, the new chip is slated to operate at speeds from 400 to 550 MHz, making it one of the fastest embedded processors announced to date. With some 23 million transistors on a 100-mm^2 die consuming 13 W at 500 MHz, the UltraSparc-IIe will also be among the largest and hottest embedded processors available—but these are likely to be acceptable characteristics for the networking, telecommunications, and mass-storage systems at which the UltraSparc-IIe is aimed.

Sun has not yet disclosed pricing for the new chip, which will come in a 370-contact plastic PGA. According to Sun's road map, the 400-MHz version will ship this year and faster parts will be available next year. —*P.N.G.* M