by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,835,968

Apparatus for providing memory and register operands concurrently to functional units
Filed: April 17, 1996 Issued: November 10, 1998
Assignee: AMD Claims: 16
Inventors: Rupaka Mahalingaiah et al.
Apparatus and methods which include at least two address generation units and corresponding reservation stations and a speculative register file. The address generation units are responsible for providing a memory address of operands based on register value components of the memory address. The speculative register file stores speculative register values corresponding to previously decoded instructions. If the register operands included in the address operands of an instruction are stored in the speculative register file, the address generation unit generates a speculative memory address while the actual operands are requested from a real register file and reorder buffer.

5,832,293

Processor architecture providing speculative, out of order execution of instructions and trap handling
Filed: August 15, 1997 Issued: November 3, 1998
Assignee: Hyundai Claims: 12
Inventors: Valeri Popescu et al.
A superscalar, out-of-order-microprocessor with register renaming. The microprocessor has branch-prediction for conditional branches and in-order instruction retirement. Traps that may occur as the result of the execution of an instruction are saved with the result of the execution of the instruction, so upon the in-order retirement of the instruction, the trap is generated, producing in-order traps.

5,832,292

High-performance superscalar-based computer system with out-of-order instruction execution and concurrent results distribution
Filed: September 23, 1996 Issued: November 3, 1998
Assignee: Seiko Epson Claims: 20
Inventors: Le Trong Nguyen et al.
A superscalar processor and methods for superscalar operation. The processor and methods describe an out-of-order processor, including storing data into either temporary or architectural registers and functional units simultaneously; performing simultaneous operations out of order, concurrently distributing the results to either temporary registers, if the operation is completed out of order or the architectural registers if the operation is completed in order.

5,828,868

Processor having execution core sections operating at different clock rates
Filed: November 13, 1996 Issued: October 27, 1998
Assignee: Intel Claims: 4
Inventors: David Sager et al.
A microprocessor with an execution-core section, including at least logical AND and OR functions clocked at a frequency at least 1.5 times faster than a second core section. The second core section includes at least a multiplier and shifter, which in turn are clocked differently (and presumably faster) than a third core section. The third core section includes at least the instruction fetcher and decoder.

5,826,089

Instruction translation unit configured to translate from a first instruction set to a second instruction set
Filed: January 4, 1996 Issued: October 20, 1998
Assignee: AMD Claims: 10
Inventor: Mark Ireton
An instruction-translation unit is disclosed that reduces CISC instructions to a set of intermediate atomic operations. The atomic operations are then recombined into instructions in a target instruction set. An execution core executes instructions of the target instruction set while maintaining compatibility with the CISC instructions. By reducing multiple CISC instructions into atomic operations, portions of multiple CISC instructions may be combined into target instructions to increase execution efficiency.

5,826,054

Compressed instruction format for use in a VLIW processor
Filed: May 15, 1995 Issued: October 20, 1998
Assignee: Philips Claims: 20
Inventors: Eino Jacobs et al.
A compressed instruction format for a VLIW processor. Instructions are byte aligned and variable length. Branch targets are uncompressed. Format bits specify how many issue slots are used in a following instruction. Instructions are stored in compressed form in memory and in cache and are decompressed on the fly after being read from the cache.

OTHER ISSUED PATENTS

5,835,782 *Packed/add and packed subtract operations*
5,829,025 *Computer system and method of allocating cache memories in a multilevel cache hierarchy utilizing a locality hint within an instruction*
5,826,055 *System and method for retiring instructions in a superscalar microprocessor* M