# A GLANCE At Microprocessor Forum, Intel described the microarchitecture of Merced, the first IA-64 chip, due mid-2000. The statically-scheduled six-issue design moves much of the complexity of superscalar processors into the compiler, allowing more transistors to be put toward instruction-level parallelism. Editorial: Intel Commoditizes 3D Graphics......3 Although discrete 3D accelerators remain the undisputed performance leaders, Intel is taking advantage of the absence of a compelling need for 3D performance to replace most of them with its own lower-cost integrated-graphics chip sets. Athlon is first PC processor to 700 MHz; Mobile Celeron jumps ahead of Pentium II; Mobile K6-2P/IIIP gain speed, market share; Rise revisits roadmap; Nvidia allies with ALi on integrated chip set; USB 2.0 speed goal raised; K8 loses architect. Taking a different route to server performance than Intel is with Merced, IBM's next-generation servers will rely on chip multiprocessing and unprecedented memory bandwidth rather than on a new instruction set. In a 4.5"-square package, Power4 will pack eight processors and hundreds of gigabytes per second of bandwidth. IBM, C-Port network processors challenge Intel; Triscend ships first reconfigurable 8051, MIPS32 4Km core has fast MAC. Motorola has combined its StarCore SC140 core with its Power-Quicc II protocol-processing engine to create the first network DSP. Targeting multimedia SOCs, Hitachi and ST are adding two hundred 32-bit instructions and sixty-four 64-bit registers to SH-5 to create a core that delivers 2.8 GFLOPS and 1.6 billion integer-MAC/s. In a bold effort to replace ASICs, Cradle has developed a "Universal Microsystem" combining a parallel array of microprocessors, DSPs, and I/O protocol engines with RAM-based PLDs to drive the pins. Replacing the venerable 440BX, Intel's new 820 chip set will improve P III performance with a 133-MHz bus, Direct RDRAMs, and $4 \times AGP$ .

The Slater Perspective will return in the next issue.

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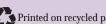
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