AT A GLANCE Intel introduces its 0.18-micron Pentium III, code-named Coppermine, into the performance PC, mobile, and workstation segments at speeds up to 733 MHz. An on-chip 256K cache reduces cost and improves performance by a full speed grade on most applications. While Intel and HP spend their efforts developing a new ISA to exploit instruction-level parallelism, other vendors are sticking with their existing ISA and focusing on thread-level parallelism instead. Infrastructure issues slow Athlon ramp in Q3; Merced becomes Itanium; ATI Mobility moves to 128 bits. Embedded News 5 Massana's DSP coprocessor bolts onto CPUs; ADI adopts AMBA for new DSPs. Motorola's next-generation PowerPC processor with AltiVec will use a longer pipeline to reach speeds of more than 700 MHz. It also sports a 22-GByte/s 256K on-chip L2 cache. IBM's forthcoming two-way superscalar core for high-end embedded applications will deliver 1,000 MIPS at 555 MHz. With its new MAJC-5200, Sun goes after thread-level parallelism with a two-core chip multiprocessor enhanced for Java execution. The Mips 5Kc, the first implementation of the MIPS64 ISA, is the first synthesizable 64-bit processor core from any vendor. AMD will use a high-speed link called LDT to connect up to eight Athlon processors and I/O bridges. The company has also disclosed plans to add 64-bit extensions to its future SledgeHammer CPU. Intel 840 Brings RDRAM to Workstations 28 Intel's new 840 chip set is the first workstation core logic to support both dual Direct RDRAM channels and 4× AGP. Mitsubishi has disclosed its next-generation volume-rendering accelerator with twice the performance of the current vg500. The Slater Perspective: Direct RDRAM (Almost) Arrives in PCs . . . 31 With its strongest benefits still in the future, Direct Rambus DRAM is struggling to gain a foothold in today's PC market. Recent IC Announcements will return in the next issue.

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