

by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send email to belgard@umunhum.stanford.edu with comments or questions.

5,898,882

*Method and system for enhanced instruction dispatch in a superscalar processor system utilizing independently accessed intermediate storage*

Filed: January 8, 1993 Issued: April 27, 1999  
 Inventors: James Kahle et al. Claims: 10  
 Assignee: IBM

A method and system for permitting instruction dispatch in a superscalar processor system. Multiple intermediate storage buffers are provided, and each time an instruction is dispatched, a specific storage buffer is assigned to any destination operand within the dispatched instruction. This permits the instruction to be dispatched within a single cycle by eliminating any requirement for determining and selecting the specified architectural register or a designated alternate architectural register.

5,898,849

*Microprocessor employing local caches for functional units to store memory operands used by the functional units*

Filed: April 4, 1997 Issued: April 27, 1999  
 Inventor: Thang Tran Claims: 28  
 Assignee: AMD

A microprocessor employs a local data cache for each function unit located physically close to that function unit. The physical proximity of the local cache to the function unit which accesses it reduces the interconnect delay between the local cache and the function unit.

5,896,528

*Superscalar processor with multiple register windows and speculative return address generation*

Filed: September 1, 1995 Issue: April 20, 1999  
 Inventors: Akira Katsuno et al. Claims: 3  
 Assignee: Fujitsu

A superscalar processor with register windows. The processor includes a return prediction table that provides a speculative return program counter for a subroutine corresponding to a selected register window, prior to completion of the execution of the subroutine, in response to the value of the current window pointer.

5,896,517

*High performance processor employing background memory move mechanism*

Filed: August 18, 1997 Issued: April 20, 1999

Inventor: Peter J. Wilson Claims: 34  
 Assignee: Bull HN

The invention provides adding a background memory move (BMM) mechanism and augmenting an instruction set to include BMM instructions by which prefetching of data from main memory to a data cache are implemented. Other BMM instructions also allow determination of when such prefetches have completed.

5,895,498

*Arithmetic processor which latches data in a temporary register before the data is latched in a general purpose register*

Filed: January 31, 1997 Issued: April 20, 1999  
 Inventors: Maki Ueno et al. Claims: 18  
 Assignee: Toshiba

A data processor, has at least two types of arithmetic operations. The first type of arithmetic operation has a predetermined period. Data results from these arithmetic operations are stored directly into the register file. The second type has a longer duration. Data results from the second type of arithmetic operation are stored in temporary result registers. These result registers are written back to the register file during periods when the register-file write ports are idle.

5,893,143

*Parallel processing unit with cache memories storing NO-OP mask bits for instructions*

Filed: June 21, 1996 Issued: April 6, 1999  
 Inventors: Kazuhiko Tanaka et al. Claim: 1  
 Assignee: Hitachi

A VLIW processor has a cache configuration such that a VLIW instruction cache is allocated into two or more separate physical caches. The caches correspond to at least two of the execution resources of the instruction. When instructions are fetched from main memory into the instruction cache, each physical cache receives the part corresponding to its execution resource. If the VLIW instruction contains a NOP for a certain resource, that cache tag is set to so indicate, but space in the cache is not used.

OTHER ISSUED PATENTS

5,898,865 *Apparatus and method for predicting an end of loop for string instructions*

5,896,529 *Branch prediction based on correlation between sets of bunches of branch instructions*

5,896,522 *Selective emulation interpretation using transformed instructions*

5,896,305 *Shifter circuit for an arithmetic logic unit in a microprocessor*

5,895,503 *Address translation method and mechanism using physical address information including during a segmentation process* □