Intel Bids $1.6 Billion for DSP Communications

Communications companies are like peanuts—once you start eating them, you can't stop. Just ask Intel, which is acquiring DSP Communications (DSPC), a supplier of chip sets and software to cell-phone manufacturers, as the latest in a series of acquisitions in the communications and networking industries.

The price isn't peanuts, though. Intel is offering about $1.6 billion in cash to DSPC stockholders, which might seem like a lot of money for a company that doesn't design any DSP cores, manufacture any chips, or count the leading cell-phone manufacturers among its best customers. But appearances can be deceiving. Unlike some other high-tech companies with billion-dollar valuations, DSPC is actually shipping real products that generate a positive cash flow, and it's sharply focused on a target market.

DSPC (*www.dspc.com*) is a fabless company that integrates DSPs and cores from TI, NEC, DSP Group, and Arm into chip sets and ASICs. The Arm cores function as microcontrollers; the DSPs handle the real work. DSPC sells the chip sets, ASICs, and related software to cell-phone manufacturers—mostly second-tier makers such as Kyocera and Philips. Leading manufacturers such as Ericsson, Motorola, and Nokia either have other suppliers or make their own parts.

Nevertheless, DSPC does a lively business ($119 million in revenue for the first three quarters of this year, a 34% increase over the same period in 1998) and isn't distracted by other markets. Intel could have gained similar technology by acquiring a company such as Philips or TI, but they are much larger, more diversified conglomerates that would have cost far more money and come with too much baggage.

Related Intel acquisitions in recent years include Case Technology, Dayna, Dialogic, IPivot, Level One, NetBoost, Shiva, Softcom, and XLNT Networks. When Intel announced its IXP1200 network processor in September (see MPR 9/13/99, p. 1), the company said it would refocus its $3.5 billion investment portfolio on communications. The DSPC acquisition is the first major result of that strategy.

Intel's recent partnership with Analog Devices (see MPR 2/15/99, p. 5) to develop a new DSP core for embedded applications is another piece of this puzzle. Clearly, Intel is looking for new avenues of growth beyond the PC market, where prices are rapidly plunging. Like numerous other companies, Intel anticipates a future of mobile, connected information appliances, and it is maneuvering to become a leading supplier for these devices. —*T.R.H.*

Motorola's DragonBall Rolls Faster

Normally it isn't big news when Motorola nudges up the clock frequency of a 68K-series microprocessor. But the company's recent announcement of a faster DragonBall chip with an integrated color-LCD controller provoked a spate of news reports about 3Com's alleged plans to introduce a new Palm organizer with a color screen. Those reports gained momentum when 3Com released a beta copy of the new PalmOS, with color APIs. But 3Com has now squashed those rumors, saying that Palm won't use a color LCD until it can do so without seriously compromising the product's size, weight, and battery life. Still, other PalmOS licensees are free to do as they wish.

The new DragonBall 68VZ328 is definitely an improvement over existing DragonBall chips—both the 68328 in the original PalmPilot and the 68EZ328 in newer models from 3Com and startup Handspring. The DragonBall VZ doubles the clock frequency to 33 MHz, adds color capability to the integrated LCD controller, adds support for SDRAM to the integrated memory controller, and has other enhancements. The table below compares the features of these chips.

Feature	DragonBall VZ	DragonBall EZ	DragonBall
Core Frequency	33 MHz	16.5, 20 MHz	16.5 MHz
LCD Controller	256 colors	16 grays	4 grays
DRAM Controller	SDRAM	EDO, FPM	None
SPI Ports	2	1	2
UARTs	2	1	1
Timers	2	1	1
PWM Outputs	2	1	1
Dhrystone 2.1	5.4 MIPS	2.7–3.2 MIPS	2.7 MIPS
Core Voltage	2.7–3.3 V	3.0–3.6 V	3.0–5.0 V
Power (typical)	54–66 mW	45–54 mW	45–75 mW
Price (10K)	$11	$8.50, $10	$10
Availability	Jan '00	Now	Now

At 33 MHz, power consumption increases to about 60 mW at 3 V (nominal), but that's a fair trade for boosting DragonBall's anemic performance to 5.4 Dhrystone 2.1 MIPS. DragonBall processors may not be speed demons, but they aren't light bulbs either.

At a bargain-basement price of $11 in 10,000-unit quantities, DragonBall VZ costs only $1 more than the new 20-MHz version of DragonBall EZ that Motorola announced at the same time. The current 16.5-MHz DragonBall EZ costs $8.50, while the original DragonBall (also clocked at 16.5 MHz) is $10. Motorola is sampling the VZ now and plans to ship production volumes in January.

Although 3Com isn't the only customer for DragonBall—the chip is also found in pagers, and more than five million have been sold—it's difficult to believe that Motorola would make so many improvements unless a major customer asked for them. Even if 3Com has no current plans to make a Palm organizer with a color screen, one of 3Com's PalmOS licensees is almost certain to seize this opportunity to differentiate its products with a feature that many Palm users desire. —*T.R.H.*

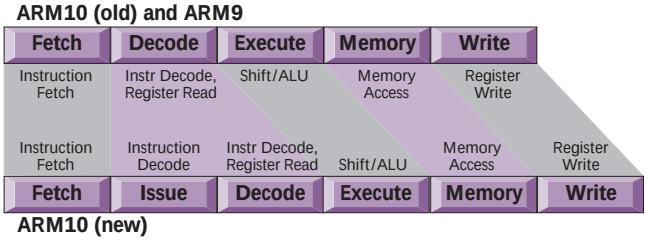
Arm Extends Reach of ARM10 Pipeline

Unable to attain its ambitious frequency goals with the original five-stage pipeline, Arm has extended the ARM10's pipeline to six stages. Arm recently taped out the new core and plans to make it available to licensees on schedule in 2Q00.

When first disclosed last year (see MPR 11/16/98, p. 14), the ARM10 core retained the same basic five-stage pipeline used in the ARM9. At that time, Arm hoped to reach its goals of 300 MHz and 420 Dhrystone 2.1 MIPS by optimizing the hard-wired logic in each pipe stage.

ARM processors require some stages to do heavy lifting. In the ARM9 and ARM10, for instance, the execute stage must perform a shift-and-add operation and check if the result is zero in a single clock cycle. (The ability to perform a shift and an ALU operation with a single instruction is a hallmark of the architecture.) The ARM9 performs those operations rapidly but sequentially; the ARM10 has additional logic to perform the zero check in parallel with the shift and add. The ARM10 also has new dedicated adders for calculating addresses while the main adder is busy with other tasks.

At first, Arm thought it could achieve its frequency and performance goals for the ARM10 by pipe-stage optimizations alone. The architects evidently ran into difficulties, because they have broken the old decode stage in two, as shown in the figure below. Arm calls the extra stage an "issue" stage, but a pipeline diagram in a preliminary technical manual indicates that instruction decoding also begins in that stage. The following "decode" stage completes the decoding and reads operands from the registers.



As a result of this change, Arm says the core will reach its original frequency target of 300 MHz in a 0.25-micron IC process. Arm is also sticking to its estimate that the ARM10 will exceed 400 Dhrystone MIPS.

The ARM10's modified pipeline is still nominally uniscalar, but some stages can handle several instructions at a time. The issue and decode stages can handle any instruction in parallel with a predicted branch, and the execute, memory, and writeback stages can handle a subset of instructions in parallel with a predicted branch. Although the ARM10 still can't complete more than one instruction per cycle, it does provide some of the throughput benefits of a superscalar microarchitecture with less complexity. —*T.R.H.*

Zoran's Soft DSP Core Optimized for Audio

At last month's Microprocessor Forum, Zoran (*www.zoran.com*) announced a new synthesizable DSP core for audio applications. Known as Muzichord, the 32-bit fixed-point DSP has enough speed and precision to handle next-generation audio standards such as DVD audio. Zoran plans to sample the first chips based on the core in 2Q00 and make evaluation samples available to customers in June.

Zoran has been making audio and video chips since 1993, when it introduced the first single-chip AC-3 decoder. The company's product line includes 20-bit DSPs for DVD, MPEG-2, and digital theater sound (DTS) decoding. Muzichord is Zoran's highest-performance DSP core and its first 32-bit device. In addition to using Muzichord in its own application-specific standard products (ASSPs), Zoran plans to license the soft core to other companies for integration in ASICs and systems on a chip (SOCs).

While Zoran's current DSPs run at a maximum clock frequency of 54 MHz, Muzichord is expected to hit 150 MHz in a typical 0.18-micron IC process. The core has about 100,000 gates and occupies less than 2 mm^2. Zoran estimates that the typical power consumption will be 120 mW at 1.8 V. In a typical 0.25-micron process, Zoran expects Muzichord to run at 120 MHz, occupy about 3.5 mm^2, and consume 144 mW at 2.5 V.

DVD audio uses 24-bit digital sampling at 96 or 192 KHz instead of the 16-bit, 44.1-KHz sampling on today's audio CDs, which explains why Zoran is aiming for higher performance and precision. Muzichord can execute a 32×32-bit multiply-accumulate (MAC) instruction with a 72-bit temporary result in a single cycle. It can also execute a radix-2 fast-Fourier-transform butterfly in four cycles and a finite-impulse response (FIR) filter at a rate of one cycle per tap. Decoding a six-channel AC-3 audio stream requires about 20% of the core's capacity. Although it carries out all those operations with 32-bit precision, Muzichord also has a 20-bit mode for compatibility with software written for previous Zoran chips.

Zoran supplies an assembler/linker, a C compiler, a source-level debugger, and software libraries for common decoding functions, such as AC-3, MPEG-1 (Layers 1, 2, and 3), MPEG-2, Dolby Pro Logic, Dolby Digital encode and decode (Surround Sound), DTS, and high-density CD (HDCD) audio. It's a mature library that's used today in many consumer products based on Zoran's previous DSPs. All the tools will be available for Muzichord in 2Q00.

DVD audio isn't Zoran's only target market for Muzichord—a wise strategy, because DVD audio is not necessarily the heir apparent to CD audio. The higher sampling rates are incompatible with today's CD players, and only audiophiles with the best equipment will notice the improvement. Muzichord's strength is its ability to process virtually any digital-audio stream that's 24 or more bits wide, such as the audio in home-theater applications. And it's a soft core, so it's an attractive choice for media-oriented ASICs, application-specific standard products, and systems on a chip.

To aid that integration, Zoran offers a library of soft peripherals designed to work with Muzichord. These include

cache controllers, an interrupt arbiter, an I^2S (inter-IC-sound) interface, and an S/PDIF (Sony/Philips digital interface format) controller.

Muzichord joins a growing number of synthesizable DSP cores from such vendors as DSP Group, Infineon, and Massana. But Muzichord is more targeted at next-generation digital-audio applications, and Zoran's C function libraries should eliminate much of the difficult DSP programming in assembly language. —*T.R.H.*

Mips Technologies Sues Lexra Over Patents

Although Mips Technologies and Lexra settled a lawsuit last year over trademark issues and product claims, it seems their legal battles aren't over. In late October, Mips filed another lawsuit against Lexra, this time alleging patent infringement. Mips accuses Lexra of infringing on at least two and possibly as many as eleven Mips patents in the design of Lexra's synthesizable processor cores, which are mostly compatible with the MIPS architecture but less expensive to license.

Lexra cofounder and CTO Pat Hays says he was surprised by the lawsuit, because the two companies have been in negotiations over a MIPS license and have exchanged written proposals over the past several months.

Mips CEO John Bourgoin says the negotiations recently stalled over money and other issues, but he doesn't consider the negotiations closed, despite the lawsuit. "A license would be a favorable outcome," he told *Microprocessor Report*.

An unusual aspect of the lawsuit is that it cites two patents that Mips says Lexra infringed and lists nine more that Lexra may have infringed, although those nine will require "further investigation and discovery," according to the complaint.

The two patents that are the primary focus of the complaint are 4,814,976 (issued in 1989) and 5,864,703 (issued last January). Patent '976 appears to cover the MIPS unaligned load/store instructions, and patent '703 covers single-instruction, multiple-data (SIMD) technology that provides extended precision.

In their previous legal clash, Mips forced Lexra to drop the letter "R" from the names of its cores (for instance, the LXR4180 became the LX4180), and Lexra agreed not to claim its cores are "MIPS compatible." Mips insisted the Lexra cores aren't truly compatible, because they don't support the unaligned load/store instructions in hardware. Instead, Lexra traps those instructions and emulates them in software by executing a series of different instructions. Mips now appears to be arguing that Lexra is infringing on Mips's patents even by emulating the unaligned load/store instructions in software. —*T.R.H.*