DSP

An open systems approach to real-time signal processing using AltiVec technology. AltiVec is a powerful new computing resource for real-time signal processing. In order to access the resource in a reasonable manner it must be incorporated into an open system architecture. Richard Jaenicke, Mercury Computer; *RTC*, 9/99, p. 47, 4 pp.

DSP apps fill out with new high-end DSP processors. Advanced VLIW, SIMD DSPs—TI's C6x, ADI's Hammerhead, Motorola/Lucent's StarCore, Motorola's G4 PPC—begin to fill the applications channel. Ray Weiss, *RTC*, 9/99, p. 19, 7 pp.

IC DESIGN

Rolling your own microprocessor. With all the options available in the world of microprocessors, you might think it would be easy to find a micro to meet any need. But a custom processor sometimes turns out to be the best solution. Monte Dalrymple, *Circuit Cellar*, 9/99, p. 76, 3 pp.

Overcoming the subwavelength challenge. For the first time in chip manufacturing history, the critical crossover point, where IC feature sizes are at or below the wavelength of light of the best-in-class optical lithography equipment, has been reached. Advancement of the semiconductor industry is running up against the immutable laws of physics. Y. C. Pati, Numerical Technologies; *Fabless Forum*, 9/99, p. 32, 3 pp.

Wafer-level processing cuts chip-scale packaging cost. Chip makers hope to eliminate die-level processing, which negatively affects throughput and yields, to lower the cost of producing chip-scale packages. David Morrison, *Electronic Design*, 10/18/99, p. 29, 1 pg.

We see the future and it's copper. It is commonly believed that copper (Cu) will be offered as the mainstream silicon interconnect technology at the 0.13-micron generation. Foundries, such as UMC Group, are introducing six layers of copper interconnect with low-*k* dielectrics and advanced 0.12-micron transistors at the 0.18-micron generation. Fu-Tai Liou, UMC Group; *Fabless Forum*, 9/99, p. 26, 2 pp.

Silicon-on-insulator CMOS devices for high-performance and low-power applications. Silicon-on-insulator (SOI)-based devices have been a research theme for about two decades. In the past few years, substantial progress and improvement in the SOI substrate wafer quality and availability have made SOI CMOS a viable alternative for low-voltage, low-power, and high-performance applications. H. Komiya, Sharp; *Fabless Forum*, 9/99, p. 24, 1 pg.

Alternatives to CMOS processes promise high speeds—at a price. Though CMOS processes have yet to reach their size or performance limits, alternative processes have already carved out niche markets for themselves and appear poised to make some inroads into the mass markets. Tess Maniwa, *ISD*, 9/99, p. 17, 5 pp.

Testing system chips: methodologies and experiences. Advances in semiconductor process and design technology require new strategies for testing complex system chips. Sujit Dey, U. C. San Diego, et al.; *ISD*, 9/99, p. 36, 7 pp.

PROCESSORS

8- and 16-bit microcontrollers serve up low cost, high performance. Recipes for speed, power, and features come together more easily as 8- and 16-bit MCUs increase their reach at a cheaper price. Dave Bursky, *Electronic Design*, 10/8/99, p. 45, 11 pp.

MAJC or mirage? With the recent release of its new chip, code-named Café, Sun claims that it is leading us to the future of technology. Whether multitudes will follow this loudly self-appointed vanguard is open to question. Peter Golden, *Electronic Business*, 9/99, p. 111, 4 pp.

Multithreaded, multiprocessor architecture aims at multimedia and networking tasks. The microprocessor architecture for Java computing (MAJC) was developed based on the observation that current and future compute tasks are, and will be, very different from the benchmark tasks used to develop existing CISC and RISC processors. Dave Bursky, *Electronic Design*, 9/20/99, p. 35, 2 pp.

EDN's 26th annual microprocessor/microcontroller directory. EDN's twenty-sixth annual directory helps you keep up with changing microprocessor and microcontroller architectures. Here are more than 50 µPs. *EDN*, 9/16/99, p. 93, 57 pp.

SYSTEM DESIGN

Tool suite is strong medicine for SOC design headaches. Now that they can interconnect disparate IP blocks via a silicon backplane, designers can simplify the SOC design process. Dave Bursky, *Electronic Design*, 9/7/99, p. 37, 4 pp.

Crossing the 3-V DSP barrier means bending the rules. Technology won't let you build a true 1-V battery-operated product, but lower-voltage design offers interesting possibilities. Trudy Stetzler and Pedro Gelabert, Texas Instruments; *Electronic Design*, 10/4/99, p. 64, 5 pp.

Integrated micromachined sensors exploit mainstream processes. Improvements in MEMS processes promise the integration of mechanical structures with CMOS functions on the same chip. Ashok Bindra, *Electronic Design*, 9/20/99, p. 48, 5 pp.

The revolution in systems engineering. The process of engineering systems on a chip will transform relationships among hardware, software, and mechanical designers. Graham Hellestrand, Vast Systems Technology; *IEEE Spectrum*, 9/99, p. 43, 9 pp.

Three techniques guide radiated-emission sources. By using far-field, near-field, and common-mode techniques, you can locate EMI sources and then reduce them so you can meet EMC guidelines. Dave Sangston, Motorola Computer Group; *EDN*, 9/30/99, p. 55, 5 pp.