by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send email to belgard@umunhum.stanford.edu *with comments or questions.*

5,923,871

Multifunctional execution unit having independently operable adder and multiplier
Filed: October 18, 1996 Issued: July 13, 1999
Inventors: Valery Gorshtein et al. Claims: 22
Assignee: Elbrus
Floating-point performance in a VLIW processor is increased through concatenation of two floating-point units, one an adder and another a multiplier. The FPUs execute independently of one another, but may operate in cooperation. Some two-operand VLIW operations use the FPUs independently. Other three-operand VLIW operations use two operands in one FPU, and they use that result and the third operand in the other FPU.

5,923,862

Processor that decodes a multi-cycle instruction into single-cycle micro-instructions and schedules execution of the micro-instructions
Filed: January 28, 1997 Issued: July 13, 1999
Inventors: Le Trong Nguyen et al. Claims: 15
Assignee: Samsung
An instruction decoder decodes an instruction by creating a decode buffer entry that includes global fields, operand fields, and a set of microinstructions. A scheduler issues the microinstructions from one or more entries to the execution units for possible parallel and out-of-order execution.

5,915,117

Computer architecture for the deferral of exceptions on speculative instructions
Filed: October 13, 1997 Issued: June 22, 1999
Inventors: Jonathan Ross et al. Claims: 34
Assignee: I.D.E.A.
A system and methods for hardware deferral of exceptions in speculative operations. The methods and apparatus use a mechanism in the processor hardware to write a "deferred exception token" into an instruction's destination without generating an exception to the operating system in a process called "eager deferral." The hardware includes a control register that includes state information that allows deferral on an exception-by-exception basis.

5,915,114

Dynamic trace driven object code optimizer
Filed: February 14, 1997 Issued: June 22, 1999
Inventors: Brent McKee et al. Claims: 37
Assignee: HP
An optimizing method that provides for dynamic, real-time optimization of executable object code. The optimizer bases the optimization of object code on data gathered from execution traces collected in real time. The executable code is modified in real-time to generate optimized object code. The claims include media that contain a program that optimizes according to the method.

5,915,109

Microprocessor for processing a saturation instruction of an optional-bit length value
Filed: December 20, 1996 Issued: June 22, 1999
Inventors: Kiyoshi Nakakimura et al. Claims: 20
Assignee: Mitsubishi
A microprocessor with a saturation unit configured to saturate at an optional, specified bit width. The saturation unit optionally selects a bit width based on an input. The unit outputs either a target value, if the target value is less than the maximum value for the bit width, or the maximum for the bit width.

5,913,049

Multi-stream complex instruction set microprocessor
Filed: July 31, 1997 Issued: June 15, 1999
Inventors: Jonathan Shiell et al. Claims: 19
Assignee: TI
A microprocessor, and methods of operation, including multiple fetch streams. Each fetch stream includes an instruction-fetch unit, a decoder and a scheduler. The decoded instructions are tagged to indicate the stream from which they came. The scheduler detects interstream dependencies.

5,913,048

Dispatching instructions in a processor supporting out-of-order execution
Filed: March 31, 1997 Issued: June 15, 1999
Inventors: Hoichi Cheong et al. Claims: 16
Assignee: IBM
The invention includes methods and apparatus for issuing instructions in a superscalar, pipelined processor. The methods assign an identification tag to an instruction and dispatch the instruction, the identification tag, and source information to an execution queue.

OTHER ISSUED PATENTS

5,920,724 *Software pipelining a hyperblock loop*
5,913,050 *Method and apparatus for providing address-size backward compatibility in a processor using segmented memory* M