

Brainiacs, Speed Demons, and Farewell

Some Vendors Learn Later Than Others That Clock Speed Drives Performance



As my final editorial for this august publication, I would like to reflect on how the industry has changed—and in some ways stayed the same—since one of my earliest editorials, discussing Brainiacs and Speed Demons (see MPR 3/8/93, p. 3).

At that time, Digital's brand-new Alpha line, HP's PA-RISC, and the MIPS R4000 strove for high clock speeds, while IBM (Power), Sun (SuperSparc), and Motorola (88110) focused on high-IPC (instruction per cycle) designs. In 1993, Speed Demons used simple scalar or two-issue designs running at 100 to 200 MHz in state-of-the-art 0.8-micron IC processes; Brainiacs could issue three or four instructions per cycle but at no more than 66 MHz.

In the subsequent seven years, better IC processes have greatly improved both the IPC and the cycle time of microprocessors, leading some vendors to claim to deliver the best of both worlds. But a chip becomes a Speed Demon through microarchitecture design philosophy, not IC process gains. The Speed Demon philosophy is best summed up by an Alpha designer who said that a processor's cycle time should be the minimum required to cycle an ALU and pass the result to the next instruction. The processor can implement any amount of complexity so long as it doesn't compromise this primary goal of ultimate speed.

One thing hasn't changed: Speed Demons still deliver the best performance. In fact, all high-end microprocessor vendors have adopted the Speed Demon philosophy to a large degree. In 1993, the clock-speed gap between the fastest SuperSparc and the fastest Alpha chip was 5×. Today, the gap between the slowest processor family and the fastest is 2.5× (see MPR 12/27/99, p. 1), with one exception: IBM's Power3.

IBM is the last bastion of the pure Brainiac approach, and its 200-MHz Power3 delivers one-third the SPECint95 performance of the 700-MHz Alpha 21264, despite using similar IC processes and a larger die. The extra transistors in the IBM design boost IPC, but by far less than the tremendous difference in clock speed required by the more complex design. It's no wonder Big Blue adopted the Speed Demon approach for its 1-GHz Power4.

What about x86 processors? AMD took the Brainiac route with its K5 design, which flopped both in performance and in the market. After that debacle, the company hired key Alpha designers to bring the Speed Demon philosophy to the K7. As a result, the K7 achieves better clock speeds than Intel's Pentium III in similar IC processes as well as better core CPU performance.

Intel edged toward the Speed Demon camp with its highly pipelined P6 core, and the forthcoming Willamette appears to be a pure Speed Demon design, targeting the same 1-GHz mark as other leading-edge 0.18-micron processors. Now that Intel and AMD have focused on clock speed, their chips deliver better performance than Brainiac RISC processors, proving that being a Speed Demon is more important than being RISC.

Like the old K5, Rise's mP6 collapsed under the weight of its Brainiac design. Cyrix's 6x86 core also failed the Speed Demon test and, after being purchased by Via, appears destined for the dustbin. Glenn Henry, head of the Centaur team, has been a strong proponent of the Speed Demon philosophy, but his WinChips have been hampered by poor IC processes. If new owner Via can solve this problem, it should have a price/performance winner.

With its focus on instruction-level parallelism (ILP), IA-64 seems to be the ultimate Brainiac. But the Brainiac/Speed Demon debate focuses on implementation, not instruction-set architecture. One of Merced's problems is that its clock speed will not be competitive with that of other 0.18-micron processors in 2000, hampering performance. Wisely, Intel has targeted the 0.18-micron McKinley at more than 1 GHz, making it a true Speed Demon. As long as IA-64 compilers can match or beat RISC compilers, McKinley will be an excellent performer.

Being a Speed Demon doesn't solve everything. For applications larger than the meager SPECint95, designers must supply adequate memory bandwidth to keep up with the fast CPU core. Speed Demons also burn more power, a problem in mobile systems. But being fast has another advantage: megahertz sell.

Over the next few years, the performance battles will be as fierce as ever, pitting Intel against a newly reinvigorated AMD and IA-64 against a plethora of RISC server processors.

I've been honored to be your commentator for the past seven years, but now it's time to sign off. In the immortal words of Douglas Adams: So long, and thanks for all the fish. ☐

Linley Gwennap is now principal analyst of The Linley Group (www.linleygroup.com). He will occasionally contribute to Microprocessor Report in the future.