by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send email to belgard@umunhum.stanford.edu *with comments or questions.*

5,930,491

Identification of related instructions resulting from external to internal translation by use of common ID field for each group
Filed: June 20, 1997 Issued: July 27, 1999
Inventors: Rolf Hilgendorf et al. Claims: 20
Assignee: IBM
A processor and methods for addressing internal instructions in an out-of-order processor with distributed reservation stations (window buffers). The processor translates from external instructions to internal instructions and may translate one to many. A common instruction identifier is assigned to all of the internal instructions within a group, which represents an external instruction in the window buffers.

5,930,490

Microprocessor configured to switch instruction sets upon detection of a plurality of consecutive instructions
Filed: January 2, 1996 Issued: July 27, 1999
Inventor: John Bartkowiak Claims: 16
Assignee: AMD
A microprocessor is configured to detect a predefined sequence of consecutive instructions. The predefined sequence indicates that subsequent instructions belong to an alternate instruction set—for example, a DSP instruction set. The number of subsequent instructions that belong to the alternate instruction set may be encoded in the instruction sequence.

5,926,832

Method and apparatus for aliasing memory data in an advanced microprocessor
Filed: September 26, 1996 Issued: July 20, 1999
Inventors: Malcolm Wing et al. Claims: 32
Assignee: Transmeta
A specific memory controller or a microprocessor with the memory controller is disclosed. The memory controller can locate or store a sequence of native instructions in memory that have been translated from corresponding target instructions by using a register. It does so in response to, among other things, determining that the sequence of native instructions is to be executed.

5,926,646

Context-dependent memory-mapped registers for transparent expansion of a register file
Filed: September 11, 1997 Issued: July 20, 1999
Inventors: James Pickett et al. Claims: 40
Assignee: AMD
A microprocessor includes an expanded set of registers in addition to the architected set of registers. The expanded set of registers is memory mapped within the context of the program but outside the architectural context save area. On a context switch, the microprocessor saves or restores the state of the expanded registers to or from the corresponding memory locations.

5,926,645

Method and system for enabling multiple store instruction completions in a processing system
Filed: July 22, 1997 Issued: July 20, 1999
Inventor: Barry Williamson Claims: 10
Assignee: IBM
A load/store unit for handling multiple store-instruction completions in a pipelined processor. The unit has at least one effective address unit, an instruction input queue, and a store queue configured such that store instructions are handled (or completed) virtually simultaneously.

5,926,642

RISC86 instruction set
Filed: May 16, 1996 Issued: July 20, 1999
Inventor: John Favor Claims: 38
Assignee: AMD
A network server that has a system bus, a LAN adapter, a PC-like bus architecture, and a superscalar processor that accept CISC instructions and implement RISC-like instructions that include a load/store class.

5,926,634

Limited run branch prediction
Filed: October 11, 1996 Issued: July 20, 1999
Inventor: David Isaman Claims: 26
Assignee: Hyundai
A prior-art branch-history predictor is augmented with two counters. The run length (consecutive "branch takens" or "branch not-takens") of a specific branch is counted in an upcounter associated with the branch. When the run length ends, the upcounter is copied into a branch-related downcounter, and the upcounter is reset. For each successive occurrence of the branch, if the downcounter is nonzero, the branch-prediction outcome is used, and the downcounter is decremented. When the downcounter is zero, the predicted outcome is complemented. When the run length of a branch history is constant, the scheme always predicts correctly.

OTHER ISSUED PATENTS

5,930,481 *System for concurrent cache data access by maintaining and selectively merging multiple ranked part …* M