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HITACHI SH7615 ADDS ETHERNET

SH-DSP Targets Net Phones, Network Devices, Modems

By Tom R. Halfhill {1/24/00-02}

To exploit the latest hot-product category—Internet gizmos—Hitachi has added an Ethernet interface and DSP instructions to one of its best-selling SuperH processors. The result is the new SH7615, which samples in March and is scheduled for volume production in June.

Although in most ways the SH7615 is a relatively minor variation of Hitachi's existing SH7604 and SH7612 chips, it brings together the critical features of network connectivity and digital-signal processing for the first time in a SuperH processor. It's designed for networking applications that normally would use a separate microcontroller, DSP, and Ethernet media-access controller.

The goal is to cut costs for network equipment, printers, voice-over-IP (VoIP) telephones, broadband modems (both cable and DSL), and a myriad of newfangled Internet appliances. SH-DSP extensions allow the SH7615 to handle such processor-intensive tasks as data compression and echo cancellation without resorting to a separate (and harder-to-program) DSP chip.

Hitachi had better step lively, though—similar processors are coming this year from other vendors, and there are also licensable cores with DSP capabilities that allow anyone to design chips like the SH7615.

SH7612 + Ethernet – 8K = SH7615

The SH7615 is based on the SH7612, which in turn is based on the SH7604, one of the best-selling chips in the SuperH line. The SH7604 was the first chip to use the SH-2 core and was designed primarily for Sega video-game consoles. It reached high volumes because there were two of them in every Genesis 32X and Saturn game machine.

Last year, Hitachi introduced the SH7612, which is basically an SH7604 with an SH-DSP core. The new SH7615

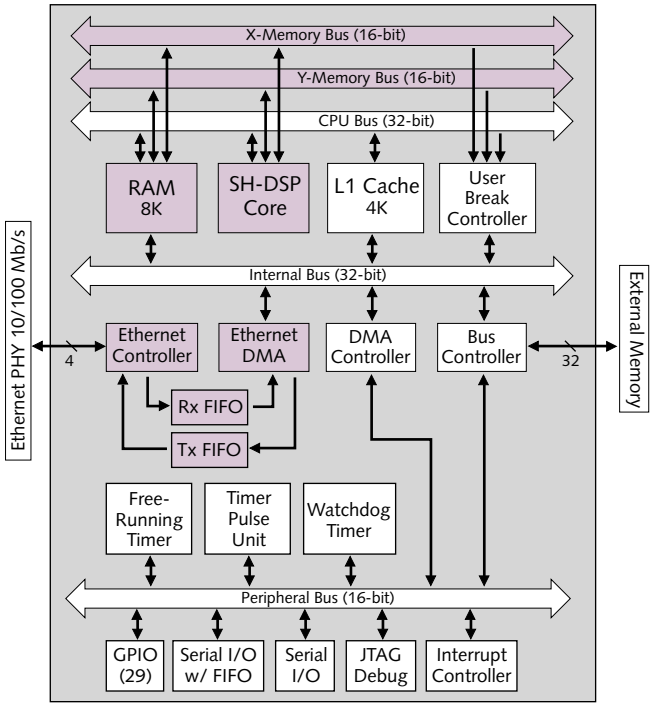

Figure 1. Hitachi's SH7615 is the first SuperH chip to integrate a network interface with DSP extensions. The Ethernet components and SH-DSP features are highlighted in purple.

pushes the evolution further by adding Ethernet support and improved I/O capabilities.

Ethernet is the main difference. As Figure 1 shows, the SH7615 has an Ethernet media-access controller that supports 10- and 100-Mb/s data rates (regular Ethernet and Fast Ethernet), two 512-byte FIFO buffers (receive and transmit), a dedicated two-channel DMA controller, and a media-independent interface to an external Ethernet PHY (physical-layer) chip.

The SH7615's Ethernet controller complies with the IEEE-802.3 standard and the HomePNA (Phoneline Networking Alliance) specification, which allows ordinary telephone lines to carry Ethernet traffic. The four-bit data interface to the PHY chip runs at 2.5 MHz for regular Ethernet or 25 MHz for Fast Ethernet.

To fully implement an Ethernet interface, the SH7615 requires only the PHY chip. (A 10-Mb/s PHY costs about $5–$6.) Depending on the number of ports on the PHY, this two-chip solution could support a four- or eight-port Ethernet switch—a low-cost device for a small business or home office. The SH7615 would also be useful in a wide variety of products that need Ethernet connectivity, such as DSL modems, cable modems, network printers, VoIP phones, Web-enabled consumer appliances, and other embedded applications.

More Taste and Less Filling

Hitachi had to provide the SH7615 with more I/O to enable the PHY interface, so the chip has 29 general-purpose I/O (GPIO) ports instead of the 14 found on the SH7612. Due to some additional I/O, power, and ground pins, this bumped the total number of leads to 208 pins instead of the 176 pins on the SH7612.

The extra pins and the Ethernet integration would have increased costs beyond the point where Hitachi felt the SH7615 would be economical for its target markets, so the designers compensated by reducing the amount of on-chip memory. The SH7615 has 8K of SRAM (not counting the 4K unified primary cache) instead of the 16K in the SH7612.

This will be a concern for embedded-system developers. The SH7615 divides the 8K of SRAM into X and Y memories for DSP operands (a familiar feature of dedicated DSPs), and Hitachi's decision to reduce the amount of SRAM will almost certainly affect performance. If a critical DSP algorithm can't find room to store its data on chip, it's the same as a cache miss—the processor must fetch the operands from slower external memory. At least the SH7615's 32-bit memory interface supports relatively fast SDRAM, as well as regular DRAM and ROM.

Hitachi will fabricate the SH7615 in a 0.35-micron three-layer-metal process. The chip has a 3.3-V core with 3.3-V I/O. (Some I/O pins tolerate 5-V signals for compatibility with 5-V PHY chips.) The relatively large geometry and 3.3-V core voltage would seem to put the SH7615 at a disadvantage against similar chips built in newer processes, such as Infineon's TriCore-based Harrier-XT, which also has an Ethernet controller and is fabricated in a 0.25-micron process. Yet the SH7615 typically consumes only 690 mW at 60 MHz—less than half as much power as the 50-MHz Harrier-XT, which has a 2.5-V core and 3.3-V I/O.

To be fair to Infineon, the Harrier-XT is more integrated than the SH7615. It has ATM, Utopia, and ADSL interfaces in addition to Ethernet, and it has much more on-chip SRAM (48K). The Infineon chip's static superscalar core can issue two instructions per cycle, while the SH7615 is limited to uniscalar execution. Still, the SH7615 is relatively miserly with power for a 3.3-V integrated device built in a 0.35-micron process, and it has various sleep and standby modes to cut power consumption further. A "magic packet" feature allows the chip to awaken from those low-power modes upon receiving a special Ethernet packet that acts as an alarm clock.

Feature	SH7615 Hitachi	SH7612 Hitachi	Harrier-XT Infineon	PPC 405GP IBM	LX5280 Lexra	ARM9E ARM	ARC 3 ARC Cores
Architecture	SuperH	SuperH	TriCore	PowerPC	MIPS-like†	ARM	ARC
Chip/Core?	Chip	Chip	Chip	Chip	Hard/Soft Core	Hard/Soft Core	Soft Core
DSP Datapath	32 bits	32 bits	32 bits	32 bits	32 bits	32 bits	32 bits
DSP Registers	6 × 32 2 × 40	6 × 32 2 × 40	16 × 32	32 × 32	32 × 32 8 × 40	14 × 32	Variable
Ethernet?	Yes	No	Yes	Yes	—	—	—
Core Freq*	60 MHz	60 MHz	50 MHz	200–266 MHz	200 MHz	160–200+ MHz	40–200 MHz
Core Voltage*	3.3 V	3.3 V	2.5 V	2.5 V	1.8 V	1.2–3.3 V	1.2–3.3 V
Power (typ)*	690 mW	690 mW	1.9 W	1.1 W (200 MHz)	225 mW	n/a	n/a
IC Process	0.35µ	0.35µ	0.25µ	0.25µ	0.18µ	0.18–0.25µ	0.18–0.35µ
Price (10K)	$28	$25	$25	$41 (200 MHz)	—	—	—
Availability	Jun-00	Now	Now	1Q00	Jan-00	1Q00	Now

Table 1. All these embedded chips and cores have fixed-point DSP capabilities, but only a few also have Ethernet controllers. ASIC developers have the option of adding an Ethernet controller to their core-based designs. *Some specifications are variable for licensed cores. †Lexra cores are mostly compatible with the MIPS architecture. n/a = data not available.

DSP Extensions Complete the Picture

The SH7615 is not a typical hybrid CPU/DSP with multiple cores like Motorola's DSP56690 (see *MPR 12/6/99-04*, "Motorola Cellular DSP Does It All"). Instead, the SH-DSP core has a fixed-point DSP unit with its own saturating-arithmetic ALU, 16-bit multiplier, barrel shifter, zero-overhead loop counters, and register file with guard bits.

The DSP unit shares everything else—such as the primary cache and address-decode unit—with the rest of the CPU and executes DSP instructions as part of a single instruction stream. The only distinction is that DSP instructions are 32 bits long, while regular SuperH instructions are 16 bits long (see *MPR 12/4/95-03*, "Hitachi Adds FP, DSP Units to SuperH Chips").

Sharing CPU resources limits the SH7615 to uniscalar execution—it cannot carry out a DSP instruction in parallel with a regular instruction. But the core is thoughtfully optimized for DSP. Thanks to the on-chip X/Y memories, dual X/Y data buses, and a five-stage pipeline, the SH7615 can fetch a 16-bit operand from each memory partition per cycle and sustain a stream of 16 × 16 → 40-bit multiply-accumulate (MAC) instructions with single-cycle throughput.

Pairing the SH-DSP core with the integrated Ethernet controller makes the SH7615 much more valuable for its target applications. In a VoIP phone, for example, the DSP unit could filter the voice-carrying packets, apply echo cancellation, and compress or decompress the voice frames. In a network printer or broadband modem, the SH-DSP instructions would be useful for compressing and decompressing data.

DSP-type extensions are becoming so generally useful that practically all embedded-processor architectures have added them in recent years. As Table 1 shows, the SH7615 has plenty of competition. But the combination of DSP extensions with Ethernet is more rare. Numerous chips, most notably Motorola's QUICC and PowerQUICC series, have Ethernet interfaces. The Motorola chips have network-protocol engines that can execute a MAC instruction, but their 68K or PowerPC cores don't have the same DSP capabilities found in Hitachi's SH-DSP.

IBM's Faster Solution

A closer rival to the SH7615 is IBM's PowerPC 405GP, which integrates both an Ethernet interface and a special function unit that executes 24 variations of MAC instructions (see *MPR 7/12/99-03*, "PowerPC 405GP Has CoreConnect Bus"). The 405GP is a considerably faster chip, running at 200–266 MHz in a 0.25-micron process, compared with only 60 MHz for the 0.35-micron SH7615. But it also burns almost twice as much power (1.1 W at 200 MHz) and costs 46% more than the Hitachi chip. The 405GP is a better solution for higher-end applications that need Ethernet and DSP, while the SH7615 is more suitable for lower-end consumer applications.

Lexra's LX5280, ARM's ARM9E, and ARC Cores' latest core have DSP extensions, generally in the form of MAC and bit-shifting instructions. All of them are licensable cores, so Ethernet integration is an option for any ASIC designer who needs it. Whether an ASIC would exceed the SH7615's combination of performance, power consumption, and price is another question—and an ASIC project that started now wouldn't be finished before the SH7615 ships in June.

The SH7615 is a useful addition to the SuperH catalog and could gain Hitachi some design wins in fast-growing product categories. Broadband Internet service is spreading rapidly in the U.S., and every DSL or cable modem needs an embedded processor and an Ethernet interface. Home networking and VoIP have equally high growth potential, expanding the market for low-cost Ethernet hubs, network-capable printers, and Internet phones.

To stay competitive in that fast-moving market, however, Hitachi needs to cut costs. A process shrink should be on the fast track. Before long, many of the products for which the SH7615 is intended will retail for under $100, so $28 for a CPU will seem a bit steep. At 0.25 or 0.18 microns, the SH7615 would cost less to manufacture. A smaller die would also allow Hitachi to restore the on-chip memory that was lost and perhaps integrate some additional components, such as a PHY chip. Still, the SH7615, as it stands today, is a good start.

Price & Availability

Hitachi plans to sample the SH7615 in March and begin volume production in June. The 60-MHz chip costs $28 in 10,000-unit quantities. For more information, go to *http://semiconductor.hitachi.com/superh/*.