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TRANSMETA UNVEILS CRUSOE

Supersecret Startup Attacks Mobile Market with VLIW, Code Morphing

By Keith Diefendorff {1/24/00-05}

After nearly five years of hiding its activities from the public, Transmeta (*www.transmeta.com*) has finally opened its kimono, revealing what it claims is an entirely new approach to x86 CPU design—the "chip" is part hardware and part software. As fascinating as the chip itself, however, is the amount of buzz Transmeta generated with its unparalleled secrecy, its big-name employees, including Linus Torvalds of Linux fame, and its heavyweight investors, such as Microsoft cofounder Paul Allen. Held in suspense for years wondering what the company would hatch, many major national and international news services swarmed over Transmeta's launch event, held in a swank villa in Saratoga (Calif.) on January 19.

Despite persistent rumors of low frequency and poor performance, the startup company has created two chips with some pretty attractive characteristics. According to company founder Dave Ditzel, the power dissipation of the Crusoe chips is typically around one watt—much less than any current mobile x86 processor from Intel, AMD, VIA, or Rise. Although Transmeta did not disclose definitive performance benchmarks, Doug Laird, vice president of product development, said that the company's high-end 700-MHz TM5400 Crusoe chip will deliver roughly the performance of a Pentium III-500 on PC applications.

If true, Transmeta may well have added enough value to capture a significant number of sockets in today's thin-and-light notebooks and tomorrow's Webpad appliances, both market niches that the company covets. In comparison, Intel's latest and greatest Mobile Pentium III, announced the same week, burns 14 W (TDP) at 650 MHz, and 8 W at 500 MHz in its low-power SpeedStep mode. Even if the TM5400 really burns 2 or 3 W at the equivalent of Intel's TDP (thermal design power), Crusoe could still claim an impressive three- or fourfold advantage in performance per watt over the Mobile Pentium III (in low-power mode). For today's ful-size notebooks, this power advantage may not be a big deal, because only about 20–40% of the power is consumed by the processor. But for the increasingly popular thin-and-light notebooks and for future Webpad devices, the processors will take a much larger portion of the power pie, making Crusoe more compelling.

To achieve these results, Transmeta pulled a couple of old techniques out of the technology grab bag: software-based instruction-set emulation and dynamic recompilation, or as Transmeta calls it, code morphing. This technique, also called just-in-time (JIT) compilation, has been banging around for many years; we can easily trace its roots as far back as to Bell Labs and IBM Research in the 1980s. Commercial x86 emulators like Sun's WABI for SPARC, Compaq's FX!32 for Alpha, and Insignia's SoftWindows and Connectix's VirtualPC for PowerPC, have advanced the state of the art, but none has provided 100% application-level compatibility and most had emulation overheads of 5:1 or worse (i.e., performance of an x86 application under emulation is one fifth of what it would be on a native x86 processor of roughly the same frequency).

Transmeta's unique twist on the emulation approach is to design the underlying microprocessor to assist the code-morphing software (CMS) layer, thus reducing the emulation penalty. Assuming Laird's performance estimate is correct, it appears the company has been very successful, losing

only about 25% in performance to emulation overhead—a huge improvement over previous attempts. We will want, however, to independently verify this performance estimate.

That Transmeta has taken this tack on emulation is not a total surprise. This approach was predictable on the basis of its patents (see *MPR 12/7/98-02*, "Transmeta Exposed") and the fact that Ditzel, before he left Sun to form Transmeta, worked closely with Russian company Elbrus (see *MPR 2/15/99-01*, "The Russians Are Coming"), which is building a processor based on similar principles. What *is* a surprise is that Transmeta claims to have achieved such a remarkably low emulation overhead.

Like Elbrus, Transmeta chose VLIW as the native architecture for its chips. Since VLIW foists off the complex instruction-reordering task to the compiler, VLIW processors can, in theory, achieve a given level of performance with fewer transistors than an out-of-order superscalar processor. Moving much of the arcane x86-architecture baggage into software also saves transistors. Since power consumption is proportional to capacitance, and capacitance to the number of transistors, the VLIW-with-code-morphing approach should require less power. Indeed, the 73-mm^2 die size of the 0.18-micron TM5400 (which includes 128K of L1 caches and 256K of L2) indicates that it may use as few as half the logic transistors of Intel's 106-mm^2 0.18-micron Pentium III.

To save even more power, Crusoe chips use what Transmeta calls LongRun power management. LongRun is similar to Intel's SpeedStep, but it allows power to be adjusted in 16 steps, compared with only two for SpeedStep. Transmeta uses run-time information gathered by the CMS to dynamically adjust the power setting from a low of 1.1 V/200 MHz to a high of 1.65 V/700 MHz. At its low-power setting, the TM5400 uses only 25% of the power that it does at the high setting. According to Transmeta, playing a DVD movie requires only about 400 MHz; on this task the TM5400 reaches a steady-state die temperature of less than half that of a Pentium III, allowing Crusoe-based systems to avoid the bulk of large heat sinks and the noise of fans.

The code-morphing approach has other benefits as well. Because the CMS is entirely RAM based, the "chip" can easily be patched in the field. Furthermore, because the instruction set used by the operating system and applications is isolated from the underlying native instruction set, Transmeta is free to redesign the architecture and microarchitecture of its future processors with no noticeable impact on user software. It's a good thing; Transmeta may need that flexibility to fix the blunder it made by not including Intel's streaming SIMD extensions (see *MPR 3/8/99-01*, "Pentium III = Pentium II + SSE") in these initial chips. The CMS approach does have one serious drawback: roughly 16M of main memory must be allocated exclusively to the CMS for caching recent x86-to-VLIW code translations. This requirement will add some cost and power to systems, though probably not much. The TM5400 employs a direct interface to SDRAM or DDR SDRAM to minimize the latency of the translation cache and system memory.

Transmeta's high-end TM5400 Crusoe chip is aimed primarily at the Windows market, while its low-end TM3120 chip is optimized for Mobile Linux–based devices. Both parts, however, are fully x86 compliant. Transmeta says that for the markets it is pursuing, x86 compatibility is crucial. Even in Webpad devices that run mostly just a browser, x86 compatibility is important to support plug-ins, which always appear first for the PC and are almost always written in x86 code. So, while x86 compatibility may not be absolutely essential, it is a very attractive feature for any processor hoping to capture a socket in a device that is adjacent to the PC in the market.

Crusoe chips will be manufactured by IBM, with which Transmeta has a foundry agreement. Transmeta says, however, that its parts were designed to be process independent and could easily be ported to other fabs if necessary. The 77-mm^2 TM3120 is being built in IBM's 0.22-micron CMOS-7S process and is available now at a price of $65 for the 333-MHz version and $89 for the 400-MHz version. The 73-mm^2 TM5400 is sampling now and is scheduled for volume delivery midyear. It will be built in IBM's leading-edge 0.18-micron CMOS-8S process and will sell for $119 for the 500-MHz version and $329 for the 700-MHz part. A number of working models and reference designs were demonstrated at the launch event, but no customers have yet come forward to declare their support for Crusoe chips. Transmeta assures us, however, that customer announcements will be forthcoming in the not too distant future.

While the Crusoe chips are not as revolutionary as Transmeta's marketing hype might lead one to believe, the company has collected a number of good ideas and engineered them into products with significant benefits in power consumption and die size. While its chips aren't as low power as some of other chips eyeing the mobile market, such as Intel's StrongARM, Transmeta's chips have the huge advantage of being x86 compatible. And compared with all other existing x86 chips from AMD, Intel, Rise, and VIA, Transmeta's chips promise a compelling power advantage that could land the company some significant design wins in notebook and Webpad devices. Transmeta's job now shifts to proving that its technology works in the real world and to staying ahead of these aggressive competitors, which are also attracted to Transmeta's chosen markets. Although its performance and compatibility claims remain to be independently verified, the company is off to a good start. ◇