PATENT WATCH

By Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send email to belgard@umunhum.stanford.edu *with comments or questions.*

5,943,493

Retargetable VLIW computer architecture and method of executing a program corresponding to the architecture

Filed: August 21, 1997 **Issued: August 24, 1999**
Inventors: Paul Teich et al. **Claims: 12**
Assignee: AMD

Methods of executing programs, and a retargetable VLIW computer, that can dynamically "swap in" instructions (and "swap out" others) that are not present as determined by a table of pointers to currently-present instructions.

5,941,983

Out-of-order execution using encoded dependencies between instructions in queues to determine stall values that control issurance [sic] *of instructions from the queues*

Filed: June 24, 1997 **Issued: August 24, 1999**
Inventors: Rajiv Gupta et al. **Claims: 20**
Assignee: HP

Instructions of a program to be executed out-of-order are compiled into separate queues along with encoded dependencies between instructions in the different queues. The processor issues instructions from each of the queues independently, except that it enforces the encoded dependencies among instructions from different queues.

5,940,626

Processor having an instruction set architecture implemented with hierarchically organized primitive operations

Filed: November 3, 1997 **Issued: August 17, 1999**
Inventor: Donald Sollars **Claims: 18**
Assignee: Teragen

A processor that logically associates snippets of primitive operations to implement an instruction set. At least one control unit sequences the associated snippets using the datapath to implement the processor's instruction set.

5,937,203

Port for fine tuning a central processing unit

Filed: September 16, 1996 **Issued: August 10, 1999**
Inventors: Sherman Lee et al. **Claims: 40**
Assignee: AMD

A tuning port in a CPU allows executing software to fine tune the CPU for better performance in real time. Some of the tuning examples given are: branch prediction policy, FPU rounding policy and operating frequency.

5,930,821

Method and apparatus for shared cache lines in split data/code caches

Filed: May 12, 1997 **Issued July 27, 1999**
Inventors: Darius Gaskins et al. **Claims: 45**
Assignee: IDT

A microprocessor with a coherent split code/data, on-chip L1 cache. The cache has cache snoop and state control connected to the data and to the code cache portions. These allow a cache line to be stored in both portions simultaneously while maintaining coherency between both instances of the line.

5,930,508

Method for storing and decoding instructions for a microprocessor having a plurality of function units

Filed: June 9, 1997 **Issued: July 27, 1999**
Inventors: Paolo Faraboschi et al. **Claims: 9**
Assignee: HP

Methods for compressing and decompressing VLIW operations into and from a VLIW instruction. A VLIW instruction is compacted by removing NOP fields, forming a compacted VLIW instruction. Function unit codes are appended to each operative field of the original instruction, and a delimiter is appended to it. NOP fields are passed over. The VLIW instructions are recreated by assigning the fields of the compressed instruction to the assigned function unit according to its code and by inserting NOPs to each function unit that did not get an assignment.

5,930,495

Method and system for processing a first instruction in a first processing environment in response to intiating [sic] *processing of a second instruction in a emulation environment*

Filed: January 13, 1997 **Issued: July 27, 1999**
Inventors: Kenneth Christopher Jr. et al. **Claims: 14**
Assignee: IBM

A processor with a native instruction set and an emulated instruction set is described. Sometimes a native instruction corresponds directly with an emulated instruction. In this case, the emulated instruction is performed by executing the corresponding native instruction using operands specified by the specific occurrences of emulated instruction.

OTHER ISSUED PATENTS

5,930,521 *Reorder buffer architecture for accessing partial word operands*

5,930,520 *Pipelining device in a parallel processing apparatus and an instruction supplying method therefor*

5,930,509 *Method and apparatus for performing binary translation*