❖ LITERATURE WATCH

BUSES

Switched fabric interconnects eagerly await InfiniBand. InfiniBand is not here yet, but module and system makers are scrambling to be ready when the new serial switch fabric interconnect technology emerges. Warren Andrews, *RTC,* 2/00, p. 16, 4 pp.

The next generation interconnect: beyond SKYchannel. The next generation of interconnect will play a very significant role in any multiprocessor system, but it must be designed to eliminate latency issues, handle increased GFLOP ratings, and provide simple error detection. Robert Hoenig and Steve Paavola, SKY Computers; *RTC,* 2/00, p. 29, 3 pp.

DEVELOPMENT TOOLS

Why tools are failing designers of deep-submicron chips. The design team and EDA tools must employ a hierarchical approach to the SoC design process. John Harrington, Lucent Technologies Microelectronics Group; *Electronic Design,* 2/7/00, p. 111, 3 pp.

IC DESIGN

10 tips for successful scan design. As gate counts increase at an enormous rate, the scan-design methodology is becoming necessary to produce high-quality chips. Ken Jaramillo and Subbu Meiyappan, Philips Semiconductors; *EDN,* 2/17/00, p. 67, 8 pp.

MEMORY

Magnetoelectronic memories last and last… Nonvolatile RAMs built with thin films of ferromagnetic material are poised to challenge dynamic and nonvolatile memories based on conventional semiconductors. Mark Johnson, Naval Research Laboratory; *IEEE Spectrum,* 2/00, p. 33, 8 pp.

Quad-data-rate SRAM subsystems maximize system performance. The latest-generation QDR SRAMs couple with an FPGA-based controller to send performance skyward. Krishna Rangasayee, Xilinx Corporation; Rajesh Manapat, Cypress Semiconductor; *Electronic Design,* 2/7/00, p. 117, 6 pp.

MISCELLANEOUS

Turbo-product codes advance ECC technology. Higher-performance ECC gives you more flexibility in defining your communication-system architecture, and turbo codes offer you improvements over older ECC algorithms. Dave Williams, Advanced Hardware Architecture; *EDN,* 2/3/00, p. 77, 5 pp.

Understanding electromagnetic fields and antenna radiation takes (almost) no math. With digital systems' ever-increasing frequencies and edge rates, electromagnetic-compatability is becoming harder to achieve and is no longer a topic just for experts. Ron Schmitt, Sensor Research and Development Corporation; *EDN,* 3/2/00, p. 77, 7 pp.

What is evolutionary computation? Taking a page from Darwin's *Origin of the Species*, computer scientists have found ways to evolve solutions to complex problems. David Fogel, Natural Selection Incorporated; *IEEE Spectrum,* 2/00, p. 26, 6 pp.

PROCESSORS

Vector unit architecture for emotion synthesis. Two vector units embedded in the Emotion Engine chip support high-quality 3D graphics, emotion synthesis, and 300MHz, 5.5-GFLOPS operation for the recently introduced PlayStation 2 game entertainment system. Atsushi Kunimatsu, Toshiba Corporation, et al.; *IEEE Micro,* 3/00, p. 40, 8 pp.

Cache memory design for Internet processors. The incorporation of hardware caches into Internet processors, combined with efficient caching algorithms, can significantly improve overall packet forwarding performance. Tzi-cker Chiueh and Prashant Pradham, State Univ. of New York at Stony Brook; *IEEE Micro,* 1/00, p. 28, 6 pp.

The MAP1000A VLIW mediaprocessor. This alternate to using custom ASICs for each multimedia processing task is a single-chip programmable media processor that also makes use of general-purpose RISC processing and a VLIW framework. Chris Basoglu et al., Equator Technologies; *IEEE Micro,* 3/00, p. 48, 12 pp.

Architectural considerations for CPU and network interface integration. An architecture for integrating communications functionality into the CPU. UNUM not only simplifies the design of communications processors but also improves their performance and provides greater flexibility. Charles Cranor et al., AT&T Labs, Research; *IEEE Micro,* 1/00, p. 18, 9 pp.

AltiVec extension to PowerPC accelerates media processing. Designed around the premise that multimedia will be the primary consumer of processing cycles in future PCs, AltiVec—which Apple calls the Velocity Engine—increases performance across a broad spectrum of media processing applications. Keith Diefendorff, *Microprocessor Report,* et al.; *IEEE Micro,* 3/00, p. 85, 11 pp.

PROGRAMMABLE LOGIC

Programmable logic expands capacity and variety. Process shrinks open new opportunities for designers. Rodney Myrvaagnes, *Electronic Products,* 2/00, p. 47, 3 pp.

SYSTEM DESIGN

Real-time software reigns in post-PC products. An RTOS is essential to untangle the complex software that you need to drive the new generation of interactive and networked embedded products. Warren Webb, *EDN,* 2/17/00, p. 95, 6 pp.