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AMD Brands Spitfire—Duron

By Kevin Krewell {5/15/00-03}

In a recent series of announcements timed to coincide with both Microsoft's WinHEC conference and its own annual shareholders meeting, AMD revealed more details of the Athlon roadmap for 2000. The value-segment processor, code-named Spitfire, has been branded Duron. (You can insert your own joke about the Duron name here.) The new Duron, which will be AMD's first Socket A processor, is expected to ship in June. AMD's other Athlon derivative for performance PCs, Thunderbird, will also ship in June. Thunderbird will be available in the Slot A form factor for OEMs only and in Socket A for the VAR/reseller channel.

The transition from Slot A to the 462-pin Socket A involves more than just a package change: AMD had to revise its implementation of the Alpha EV6 bus to make it more PC and socket friendly. AMD revised the original EV6 design, which had open-drain drivers and 50-ohm pull-up resistors at each end of the bus, with push-pull drivers and a simplified termination. The low-impedance termination/pull-up resistor design was fine for Alpha systems, where power, board space, and cost are less important. For PCs, however, push-pull drivers simplify board layout, reduce board space requirements, and reduce the component count, all without sacrificing performance; these considerations are especially important in value and mobile designs.

Unfortunately, this bus change necessitates new chip sets from both AMD and VIA. AMD will provide a new version of the AMD-751 (Irongate) north bridge, and VIA will ship the KT-133 chip set to replace the KX-133. AMD has also revealed that VIA's KX-133 will not be compatible with Slot A versions of Thunderbird, which means that motherboards now in the channel will not be compatible with Thunderbird. This problem should not impact AMD's OEM customers, because their designs are all based on the AMD-751 north bridge, which will work with Slot A Thunderbirds.

AMD has stated that Duron will have more total on-chip cache than Intel's Celeron, but we expect the design to be unorthodox. Intel's Celeron has relatively small L1 caches (16K for data and 16K for instructions) and a medium-size 128K L2. In contrast, the Athlon core has relatively large L1s (64K for data and 64K for instructions). Normal cache-design practice would call for an L2 that is considerably larger than the L1s, indicating a 256K or larger L2 for Athlon. Indeed, AMD has revealed that Thunderbird will have a 256K L2. Duron, however, is targeted at the value segment and would not be economical with 384K of on-chip cache, because it would grow the die from the current 102mm^2 to about 130mm^2. AMD needs to keep Duron's manufacturing cost closer to that of Intel's Celeron, which has a 106mm^2 die size. We believe AMD gave Duron a much smaller, 64K, L2 cache to resolve this quandary and keep it competitive with Celeron on cost and performance. We estimate that the small L2 cache, along with some repacking of the core, will hold the die size under 110mm^2. Duron will allow AMD to compete very effectively with Intel's Celeron in both price and performance.

It is nearly unheard of for a processor to have an L2 cache smaller than its L1, yet that is what we expect AMD to do with Duron. To maximize the efficacy of such an unusually small L2, AMD will use an exclusivity policy. In an exclusive cache, the L2 stores only data and instructions that are not in the L1, usually after the cache lines have been

evicted from the L1. Inclusive caches, on the other hand, load data into both the L1 and L2 for simplicity. Despite its unusual design, Duron will still offer a total of 192K of on-chip cache versus 160K for Celeron. We expect AMD to market Duron's total amount of on-chip cache, rather than just the L2 cache size, for obvious reasons.

Technically, a 64K L2 cache violates Microsoft's PC99 specification, which specifies 128K of L2 for office and consumer PCs. Meeting the PC99 standard is required to pass the Windows Hardware Quality Lab (WHQL) certification and to get Microsoft's logo ("Designed for Windows"). Considering that the language for the proposed PC2001 specification mentions 128K of cache, not specifically L2 cache, and that Duron has 128K of L1, we expect Microsoft will have no problem with Duron.

The forthcoming mobile version of Athlon was previously indistinguishable from the workstation/server version, with both products being called Mustang. Now AMD has separated their identities by giving the mobile version a new code name—Corvette. The new name continues AMD's car-oriented code-name scheme. Mustang is now shown on AMD's processor roadmap with a large (up to 1M) on-chip cache, which could be sold under the Athlon Ultra brand, and a mainstream version, which would presumably replace Thunderbird.

The large-cache version of Mustang will be AMD's first serious entry into the workstation and server markets, and its launch should coincide with AMD's first production dual-processor chip set. The dual-processor chip set is based on the single-processor AMD-760 north bridge that AMD demonstrated at WinHEC 2000, which supports DDR memory and AGP 4x. The parts are so similar that the multiprocessor chip set will be named the AMD-760MP. These new chip sets will finally provide the system bandwidth to match the processor's 1.6GB/s bus.

The next step in the process of morphing Athlon from a performance-PC processor to a value-PC processor will be chip sets with integrated graphics. We expect those chip sets in 2H00 from vendors such as ALi, SiS, and VIA. At that time, AMD will have a complete solution to go up against Intel's Celeron and its 810e chip set. AMD does not, however, have an integrated processor on its roadmap to counter Intel's highly integrated Timna processor, which has on-chip graphics and a memory controller. AMD, at this time, is focused on its entry into the high end and on bringing Athlon Ultra to market at the end of this year. It will probably leave the fight for the very low end, highly integrated processor market to Intel and VIA, at least for a while.