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DURON TAKES ON CELERON

AMD Deploys On-Chip L2 Across Athlon Product Line

By Kevin Krewell {6/26/00-02}

AMD recently introduced the Thunderbird-based Athlon processor during the Computex show in Taiwan (see *MPR 06/12/00-04*, "Athlon Gets Thunderbird Power"), and on June 19 it officially launched Duron (see *MPR 05/15/00-03*, "AMD Brands Spitfire—Duron") at the PC Expo show in New York City. Both AMD processors add on-chip L2 cache to the Athlon core, making them more formidable competitors to Intel's Pentium III and Celeron. In retrospect, the launch sites appear to be backward. Thunderbird, which will target the commercial market, would have been better suited to an announcement in New York City, which is associated with major corporations and Wall Street financial institutions. Duron, which was designed for economy, seems to be more closely associated with the role of the Taiwanese infrastructure.

Duron, which is shown in Figure 1, and Thunderbird should provide the majority of AMD's processors for the second half of 2000 as the Socket7-based K6-2 and the current off-chip-cache version of Athlon (K75) ramp down. AMD has no plans to sell the 0.18-micron K6-2+ into desktop applications, but it will continue to manufacture the K6-2 in 0.25-micron for the desktop. The 0.18-micron K6-2+ and K6-III+ processors will be used exclusively for Mobile applications as AMD attempts to hold onto its market share while it waits for Corvette, the mobile version of Athlon due toward the end of the year.

AMD repacked the core of Duron so that, even with the 64K on-chip L2 cache, the die is actually smaller than that of the K75 from which it is derived. The Duron processor, even at a relatively small 100mm^2, is still significantly larger than the compact 78mm^2 K6-2. Consequently, AMD may not be able to take Duron pricing much below $60, which could leave a market opportunity for VIA's Cyrix III (see *MPR 6/26/00-03*, "Cyrix III Is Dead, Long Live Cyrix"). Nonetheless, AMD had to introduce Duron at this time, as the K6 microarchitecture ran out of steam at 550MHz. Duron, because it is based on the same core as Thunderbird, should have no trouble scaling to gigahertz speeds, allowing it to easily keep pace with Intel's Celeron.

AMD won't have as much manufacturing flexibility as Intel. Since both Pentium III and Celeron use the same Coppermine die, Intel can decide at wafer-sort or die-test time which ones become Pentium IIIs and which ones become Celerons. In contrast, AMD uses a different die for each

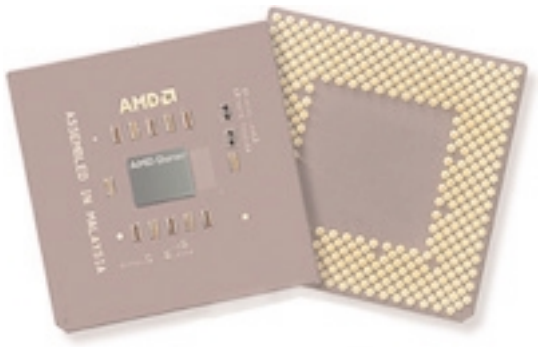

Figure 1. This photograph shows Duron in flip-chip packaging. The top of the ceramic package has a number of small jumper pads, which select default operating parameters such as processor core voltage and clock frequency multiplier.

segment, which gives it less flexibility. AMD might still be able to downsize Thunderbird's L2 to 64K and package those parts as Duron, if needed. The advantage of a market-segment-specific design is that it can be optimized for that segment.

The new Athlon has more thermal headroom than its predecessor. The maximum power dissipation of a 1GHz Thunderbird is 54W (at 1.85V), compared with the K75-based 1GHz Athlon at 65W (at 1.9V). The current requirements have dropped from 37A to 35A, and fast Thunderbirds (900–1,000MHz) run at a slightly lower core voltage of 1.75V, compared with 1.8V for the K75.

Invest Your Cache Wisely

Duron and Thunderbird represent a departure in cache design for AMD. Whereas previous cache designs—including the K6-III, K6-2+, and K6-III+—were inclusive, Duron and Thunderbird have exclusive L2 caches. In a two-level inclusive design, a cache line into L1 is also present in L2. One advantage of this design is that during a cache snoop, only the L2 tags must be interrogated.

In an exclusive design, L1 cache lines are not also present in L2. When the L1 evicts a cache line, that line is written to the L2 cache. In the Thunderbird and Duron design, on a cache line miss in the L1, if the L2 can supply the line, the line is invalidated in the L2 after being copied to the L1. The advantage of the exclusive design is that the total amount of data held in both caches is additive—in the case of Duron, that's 192K (128K+64K), and for Thunderbird, 384K (128K+256K). In an inclusive design, since the contents of the L1 are duplicated in the L2, the total effective amount of cache is only the size of the L2, which is 128K for Celeron and 256K for Pentium III. A larger cache usually increases the hit ratio in on-chip memory, improving performance.

The disadvantage of an exclusive cache, however, is that a cache snoop must look in both the L1 and L2. In a large MP system, the snoop traffic could occupy a significant amount of L1 bandwidth, reducing the amount available to the processor core. This is not a problem for Duron, which is expected to ship exclusively in single-CPU consumer platforms, and at present there are no Athlon multiprocessing chip sets to provide a measure of the performance impact. This problem may be mitigated with separate snoop tags or other tricks to avoid conflicts with the processor core, but AMD has not revealed how Thunderbird addresses this issue.

AMD also increased the hit ratio for the L2 cache on Thunderbird over K75 by making it 16-way set-associative versus 2-way. This change reduces misses caused by cache-index conflicts. Thunderbird's L2 data integrity is protected from soft-errors by error correction codes (ECC), as was the external L2 for the K75.

Socket to Me, Again

After a brief fling with slot-and-module packaging for Athlon, AMD has returned to a socket-and-PGA-package approach with the announcement of Socket A. Unlike Intel, AMD never actually left sockets behind, continuing to stick with them for the K6-2.

AMD embraced the SECC-like cartridge from Pentium II because, early in the Athlon design, it believed that Intel would eventually make the module standard for the industry. At that time, the SECC cartridge was considered an improvement over the PentiumPro and its expensive multichip module. While offering superior cache bandwidth with commodity SRAMs, the SECC-style cartridge was more expensive to manufacture than the ceramic PGA used for socketed processors like the K6. Intel recognized this fact and wisely decided to return to sockets, beginning with Socket370 for Celeron. AMD, recognizing the error of its ways in following Intel down the wrong path, has also returned to sockets. But the transition from slot to socket had an impact on the EV6 bus AMD used for Athlon.

Athlon's EV6 bus is an open-drain design that uses 47-ohm pull-ups at both ends of the transmission line for termination. This low-impedance design requires tight design rules, which result in expensive motherboard designs. The original design worked fine for the slot design (and for expensive Alpha workstations); with a socket, however, it becomes difficult to place the termination resistors sufficiently close to the processor for good transmission characteristics. AMD therefore made the bus more

Company	AMD				Intel	
Brand Name	Athlon			Duron	Pentium III	Celeron
Code Name	K7	K7	Thunderbird	Spitfire	Coppermine	Cumine-128
Process	0.25 6M, Al	0.18 6M, Al	0.18 6M, Al/Cu	0.18 6M, Al	0.18 6M, Al	0.18 6M, Al
Transistors	22 million	22 million	37 million	25 million	24 million	24 million
Die Size	184mm^2	102mm^2	120mm^2	100mm^2	106mm^2	106mm^2
L1 Cache Size	128K	128K	128K	128K	32K	32K
L2 Cache Size	512K, off-chip	512K, off-chip	256K, on-chip	64K, on-chip	256K, on-chip	128K, on-chip
L2 Organization	2-way	2-way	16-way	16-way	8-way	8-way
L2 Divisor	1:2	1:2-1:3	1:1	1:1	1:2	1:2
L2 Data Path	64-bit	64-bit	64-bit	64-bit	256-bit	256-bit
Caching Policy	Inclusive	Inclusive	Exclusive	Exclusive	Inclusive†	Inclusive†
Infrastructure	Slot A	Slot A	Slot A/Socket A	Socket A	Slot 1	Socket 370
Price Range*	—	$183–$990	$319–$990	$112–$192	$193–$990	$79–$112

Table 1. This table summarizes the evolution of the Athlon family from its introduction. The die sizes of Athlon (Thunderbird) and Duron (Spitfire) are competitive with Intel's Coppermine (-128) die, which is used for both Pentium III and Celeron. † MDR Estimate (*Source: vendors, 1,000-unit quantities.)

cost-effective by returning to push-pull drivers and open-ended terminations, with relaxed impedance tolerances. These changes should improve motherboard manufacturing yields and lower costs significantly. Another improvement included in Socket A was the move to five voltage-identifier (VID) pins, instead of the four used in Slot A, allowing core voltages down to 1.1V (instead of 1.3V minimum in Slot A). AMD also added support for a 133MHz system clock in Socket A, which will allow it to introduce a 266MHz front-side bus in 2H00.

During the transition to Socket A, AMD will continue to offer, to its OEM customers only, Thunderbird in a Slot A module. In the module version, Thunderbird runs with the original open-drain EV6 bus. AMD plans to move Athlon to Socket A exclusively as soon as OEMs can accommodate the newer design. The VAR channel will not be afforded the same luxury and will have to choose between K75 Athlon in Slot A or a move to Socket A for Thunderbird and Duron.

Infrastructure: Athlon's Achilles' Heel

At launch, chip-set support for Thunderbird and Duron include the aged AMD-750 and the VIA KT-133. AMD will continue to sell the 750 to support OEM customers and to supplement VIA chip sets in the channel, but it would prefer to drop the 750 and leave the business to third parties. Unfortunately, the third parties have, so far, provided only mediocre support for Athlon. SiS has announced a new fully integrated chip set, scheduled to ship in August, and ALi is expected to deliver a DDR chip set in 2H00—both more than a year after Athlon began shipping. Rather than embrace Athlon, third-party vendors appear to have taken a wait-and-see attitude—waiting for AMD to ramp to sufficient volume and garner sufficient OEM support—before committing the resources to get an Athlon chip set to market. SiS and VIA both offered chip sets with advanced features for the Intel P6 bus (the SiS630 and ApolloPro133A, respectively) first, before offering a Slot A or Socket A version (SiS730S and KX133). This less than enthusiastic support has left Athlon trailing Pentium III on advanced system features.

VIA, in particular, is an interesting case. VIA sells processors that compete with AMD in the value segment (Cyrix III), and yet it also provides AMD with a key system component—the KT133 chip set. At the moment, the KT 133 is the only shipping Athlon chip set that supports modern system features such as PC133 memory and AGP 4x. Meanwhile, VIA introduced an integrated chip-set design for Intel processors based on the S3 Savage4 graphics core—the SavagePro PM133 (See *MPR 05/15/00-04*, "S3-VIA Debuts Integrated-3D Chip Set")—that is not yet available for Socket A.

AMD's first opportunity to take a lead position is with the introduction of double-data-rate (DDR) SDRAM chip sets from ALi and its own 760. Until that time, we will not see the full performance benefit of the Athlon front-side bus. The current Athlon bus has a bandwidth of roughly 1.6GB/s, but PC133 SDRAM can supply at most 1GB/s, which must also be shared with the PCI and AGP channels. When DDR-266 arrives, AMD will speed up the Athlon bus to 266MHz to balance processor and memory bandwidths. Chip-set designs are also easier to design and perform better when the processor and memory operate at multiples of the same clock. We expect Athlon performance to improve somewhat with the faster bus, but the real benefit will be realized when higher clock speeds are available in the post-GHz era. The faster front-side bus will reduce the ratio of the processor-to-external-bus frequencies and reduce the time the CPU is stalled on cache misses.

AMD expects to have dual-processor support for Athlon in late 2000, when it ships the 760MP. Until then, AMD's multiprocessing support is stalled. AMD expects multiprocessor chip-set support from Alpha Processors Inc. (API) and Micron, but no schedules have been announced, and API's strategy remains unclear. Another potential supplier, Hot Rail, has already bailed out of chip sets (see *MPR 5/22/00-03*, "HotRail Derails Chip Set"). While Ali, SiS, and VIA are competent enough to supply consumer systems, they are not serious about the low-volume workstation and server markets. What AMD needs is a chip-set vendor such as ServerWorks to help it in the server segment. Micron could deliver the right support, but we believe AMD must also have the ability to control its infrastructure and meet its strategic goals with in-house silicon. Intel learned years ago that there was more to the PC processor business than just fast processors. AMD appears still to be struggling with that lesson.

Benchmarks Show Improvements

AMD has revealed that the 1GHz Thunderbird scores a 290 SPEC2000fp (base), with assistance of Compaq's Fortran compiler, which we estimate to be about 15%–20% faster than K75. The 290 score tops Intel's 1GHz Pentium III score of 273 by a solid 6%. But although AMD has published a number of general-purpose system benchmarks, it has yet to publish a SPEC2000int number. The target is the 1GHz Pentium III, which scores 407 SPEC2000int (base) on Intel's VC820 platform.

If AMD wants to address the server and workstation market segments, which are "stage two" of AMD CEO Jerry Sanders' three-stage plan (where "stage one" is the PC market and "stage three" is the information appliance market), AMD has to learn to play with the big boys and publish SPEC numbers in a timely fashion. AMD didn't publish SPEC2000 results for K75, because it faired poorly against Pentium III. The delays in releasing SPEC2000 results for Thunderbird are probably due to continual tweaking of the benchmark to get the absolutely best possible score.

AMD must get over the need to win every benchmark and adjust to the real world, where it won't win every time.

Price & Availability

The new Athlon and Duron processors are shipping now. The Athlon prices are $990 for 1GHZ, $759 for 950MHz, $589 for 900MHz, $507 for 850MHz, $359 for 800MHz, and $319 for 750MHz. Duron is priced at $192 for 700MHz, $154 for 650MHz, and $112 for 600MHz. All prices are for 1,000-unit quantities.

This will be especially important as it attempts to move beyond the shrill marketing of consumer PCs into the more sedate world of commercial customers. In the server market, as Sun has amply shown, success does not require the best benchmark scores. That said, the new Athlon benchmarks very competitively with Intel's Pentium III, up to and including 1GHz speeds, now that it is unshackled from a slow external L2. While Thunderbird's L2 has only half the raw bandwidth of Intel's advanced transfer cache, Athlon's much larger L1 and more aggressive core should put it ahead on performance.

Duron's performance should trounce Celeron's, due to Duron's larger on-chip cache and its much faster front-side bus. Intel will have to move Celeron onto a 100MHz front-side bus to have any hopes of matching Duron's performance. In a reversal of roles, Intel will have to rely on its ability to offer less expensive, more highly integrated chip-set solutions (the 810 and 815), instead of CPU performance, to appeal to the value customer. AMD will have only one integrated chip set, from SiS, scheduled to ship in August.

Durons, Thunderbirds Are Go!

With these new chips, AMD is well positioned to continue challenging Intel on all fronts in desktop PCs, although Intel will maintain its domination in the commercial market. Intel's Achilles' heel is its reliance on Rambus memory for the high-performance systems and for its upcoming Willamette. AMD has chosen to support DDR SDRAM memory, which should give it a near-term tactical advantage. But success is not a slam-dunk; the DDR could easily run into the same signal-integrity problems Intel had with RDRAM last year. Those issues are hard to predict (just ask Intel).