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# CYRIX III IS DEAD, LONG LIVE CYRIX III

*By Keith Diefendorff {6/26/00-03}*

VIA Technologies has decided to take the dipstick approach to repairing its Cyrix III processor. (The "dipstick approach" is used on automobiles that are in such disrepair that the only way to fix them is to remove the dipstick, drive a new car underneath, and replace the dipstick.) Just three months ago, VIA CEO Wen Chi Chen announced that the Cyrix III would be based on Joshua (see *MPR 3/13/00-01*, "Joshua Becomes the VIA Cyrix III"), which was designed by its recent acquisition Cyrix (see *MPR 7/12/99-02*, "VIA to Acquire Cyrix from National").

Apparently, however, VIA has recognized problems with that part. First, at a top speed of only 433MHz, Joshua would not have been frequency competitive with the current 600MHz Celerons, despite VIA's ploy of trying to pull the wool over consumers' eyes with Cyrix's bogus performance-rating (PR) scheme. Second, at 100mm$^2$ in a National 0.18-micron process, manufacturing the part would not have been sufficiently inexpensive to allow VIA to get away with selling it at a much lower price than Celeron. Perhaps the biggest problem with Joshua, however, was that it was a dead-end design. Virtually all Cyrix engineers left the company shortly after VIA acquired Centaur, Cyrix's chief rival (see *MPR 8/23/99-msb*, "VIA Buys Centaur, Slashes Cyrix"). With no engineers left to finish the design or to enhance it in the future, the only sensible thing for VIA to do was pull the plug.

In fact, we suspect that VIA had already decided never to ship Joshua, even before it announced the Cyrix III back in February. It probably went ahead with the Joshua announcement simply as a placeholder while its new Centaur subsidiary worked feverishly on the real McCoy. Apparently, VIA wanted to wait until Centaur's new chip was fully operational and in the hands of customers before announcing the switch.

The new Cyrix III, code-named C5A by Centaur and Samuel by VIA, is based on Centaur's WinChip 4 microarchitecture (see *MPR 12/7/98-05*, "WinChip 4 Thumbs Nose at ILP") but substitutes a 133MHz P6 bus and a Celeron-compatible Socket 370 PGA package for the original Socket 7. The C5A was apparently a rush job to get the WinChip 4 core to market as quickly as possible. The design retains the 64K/64K L1 cache structure of the WinChip 4 design as well as the same pipeline design and function units. Centaur's earlier claims for this design suggest that it should perform about as well as a Celeron (cycle for cycle), except on floating-point and 3D. Sources indicate, however, that Centaur may already have taped out a more aggressive redesign (the C5B?) that adds an L2 cache and some core improvements that will bring the Cyrix III fully up to the performance level of Celeron, or perhaps slightly higher.

The C5A version of the Cyrix III will be built by TSMC in its high-performance 0.18-micron CL018LV six-layer-metal process with all-aluminum interconnects. In this process, the new Cyrix III will clock at 533MHz to 667MHz, burn less than 8W of power (typical at 533MHz), and occupy only 76mm$^2$ of silicon, which is about 30% smaller than Celeron. Given TSMC's roadmap (see *MPR 6/5/00-01*, "TSMC Sets Sights on #1"), we expect the follow-on version of the Cyrix III—the one Centaur just taped out—to use TSMC's new 0.15-micron seven-layer-metal CL015LV process with at least some layers of copper interconnect. Even with an L2, this process should bring the Cyrix III's die size down into the 50mm$^2$ range.

In quantities of 1,000 units, the Cyrix III is available now at a list price of $75 for the 533MHz version and $160 for the 667MHz version. Even if discounted heavily, with a manufacturing cost below $35 (as predicted by the MDR Cost Model), the new version of the Cyrix III should yield a comfortable profit for VIA, thanks to Centaur.