PATENT WATCH

By Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send email to belgard@arithmetic.stanford.edu *with comments or questions.*

6,044,206

Out of order instruction processing using dual memory banks

Filed: October 14, 1997 **Issued: March 28, 2000**
Inventor: Leslie Kohn **Claims: 23**
Assignee: C-Cube

A process of synchronizing two execution units sharing a common memory with dual memory banks starts by assigning each memory bank to an execution unit. Two independent operation sequences are processed by the execution units. When the first execution unit completes its sequence, a synchronizing operation is performed to suspend processing in the execution unit until the other execution unit has completed. Then the assignment of memory banks is swapped between the two execution units, thereby preventing erroneous reads and writes.

6,041,167

Method and system for reordering instructions after dispatch in a processing system

Filed: July 27, 1995 **Issued: March 21, 2000**
Inventor: Peter Song **Claims: 21**
Assignee: IBM

A particular instruction is dispatched to superscalar execution circuitry. After dispatching the particular instruction, but before finishing its execution, an "execution-serialized" instruction is dispatched to the execution circuitry. A third instruction may also be dispatched to the execution circuitry. The execution-serialized instruction must execute (as opposed to retire) in program order, as execution-serialized instructions may not use rename registers and may have no commit phase.

6,035,316

Apparatus for performing multiply-add operations on packed data

Filed: February 23, 1996 **Issued: March 7, 2000**
Inventors: Alexander Peleg et al. **Claims: 16**
Assignee: Intel

A processor with first and second registers having first and second packed data, respectively, is disclosed. Each packed data includes four elements. A multiply-add circuit is coupled to the first and second registers. The multiply-add circuit includes four multipliers. Each of the multipliers receives a corresponding set of data elements. The multiply-add circuit further includes an adder coupled to the first and second multipliers, and a second adder coupled to the third and fourth multipliers. A third register is coupled to the output of the adders. The third register has two fields for saving the output of the first and second adders as first and second data elements of resulting packed data.

6,035,122

Compiler for converting source program into object program having instruction with commit condition

Filed: May 14, 1998 **Issued: March 7, 2000**
Inventor: Hideki Ando **Claims: 1**
Assignee: Mitsubishi

A processor executes an instruction speculatively. The instruction has a commit condition, provided by a compiler to the processor, indicating a number of branch conditions. The processor includes a commit condition decoder for decoding the commit conditions, an architectural register file, a shadow register file for speculatively holding data, and a register having determination entries. Each of the determination entries holds a true/false indication corresponding to a branch condition result. Circuitry is provided to compare an instruction decode entry with the determination entry. If the determination entry matches the instruction decode entry, a commit control circuit commits the result shadow register to a corresponding architectural register.

6,035,118

Mechanism to eliminate the performance penalty of computed jump targets in a pipelined processor

Filed: June 23, 1997 **Issued: March 7, 2000**
Inventors: Gary Lauterbach et al. **Claims: 3**
Assignee: Sun

A technique for increasing the performance of jump instructions in a deeply pipelined processor includes a signal indicating that the top of the return address stack has been updated by an address moved to the return register. An instruction moving a previously computed jump target address to the return register is included in code to be executed. The pipeline speculatively uses the instruction at the top of the RAS as the target instruction of a fetched jump instruction and immediately begins fetching instructions indicated by the guess.

OTHER ISSUED PATENTS

6,035,380 *Integrated circuit*
6,032,252 *Apparatus and method for efficient loop control in a superscalar microprocessor*
6,032,241 *Fast RAM for use in an address translation circuit and method of operation*