Cahners
MICROPROCESSOR REPORT
www.MPRonline.com
THE INSIDER'S GUIDE TO MICROPROCESSOR HARDWARE

IBM Brings L2 Onto PowerPC 750

New 750CX Version of Venerable Chip Boosts Performance, Lowers Costs

By Keith Diefendorff {7/24/00-01}

At the recent **Embedded Processor Forum**, PowerPC architect Peter Sandon described IBM's newest PowerPC processor, the 750CX. The CX uses the same basic core as the 750 (G3) IBM currently sells to Apple for use in iMacs and Powerbooks (see *MPR 9/14/98-msb*, "IBM Delivers on Copper Promise With 750-400"), but the new chip includes a number of cost and performance enhancements. The most notable improvement is the addition of a 256K on-chip L2 cache, a feature made possible by the use of IBM's 0.18-micron six-layer-copper CMOS-8S process (see *MPR 9/14/98-01*, "The Race to Point One Eight").

The target market for the new processor is not just Apple's computers, however. The part is also destined for high-end embedded applications, such as communications, networking, RAID controllers, and printers. Although Apple sells millions of 750-based computers for which the CX would be a nice upgrade, it must soon (once Motorola gets its IC-process act together) convert its product line to 7400 (G4) processors, which have the superior multimedia-handling capabilities necessary to compete in the PC market. Motorola is also working to enhance its 7400 with an on-chip L2, as well as with a longer pipeline for higher frequencies (see *MPR 10/25/99-02*, "PowerPC G4 Gains Velocity"). Even after Apple converts to G4s, however, IBM expects to have a large market for the 750CX, which is one of the highest-performance general-purpose embedded processors available.

Building on the 750 Core

Like the 750 (see *MPR 2/17/97-03,* "Arthur Revitalizes PowerPC Line"), the CX is a two-issue (plus one folded branch) out-of-order superscalar processor with a four-stage pipeline, two full integer ALUs, and a powerful floating-point multiply-add unit. The FPU in the CX is

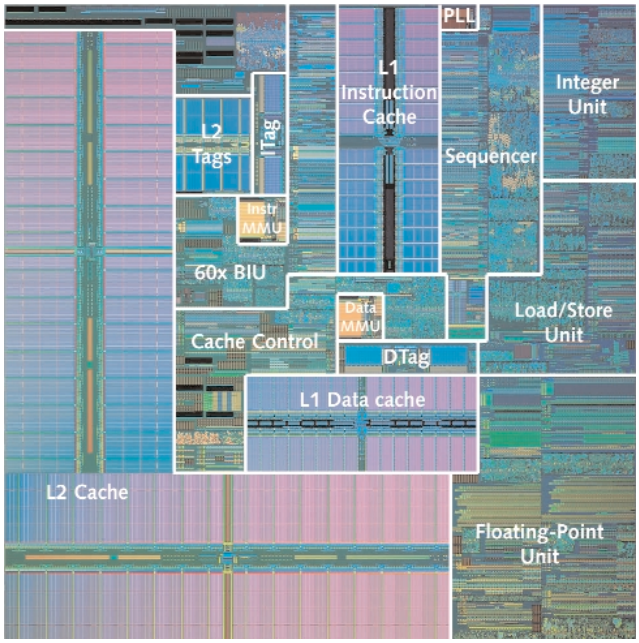
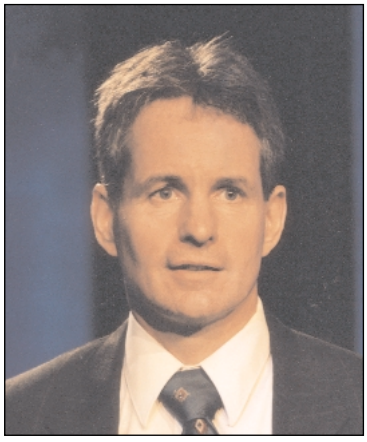


Figure 1. The 21.5-million-transistor 750CX occupies a mere 42.7mm^2 of silicon in IBM's 0.18-micron six-layer-copper CMOS-8S process. Even with its 256K L2 cache, the CX die is not much larger than the 40mm^2 750.

enhanced slightly over that in the 750 by the addition of a second reservation station. This feature allows the FPU to attain an issue rate of one floating-point instruction per cycle in most cases, even though double-precision multiplies require two passes through the multiplier. Sandon says the second reservation station improves performance on floating-point-intensive loops by as much as 12% over the 750 at the same frequency.

IBM also increased from 8 bits to 12 bits the accuracy of floating-point reciprocal estimates, an improvement that reduces the number of Newton-Raphson iterations required to produce a full-precision reciprocal. This method of performing division is especially effective on the PowerPC because of its fused multiply-add operations. The speedup from the higher-precision reciprocal estimate (seed) should significantly improve, among other things, 3D-graphics normalization operations.

The 64-entry branch-target cache and the 512-entry branch history table are unchanged from those in the 750. Also unchanged are the dual 32K eight-way set-associative L1 caches and the dual 128-entry two-way set-associative TLBs. The width of the L1 data-cache-reload path, however, was increased from 64 bits to 256 bits in order to reduce contention for the L1 between the bus and the load-store unit. The CX uses the same 60x bus as the 750, supporting half-integer bus dividers between 2x and 10x but limited to a top speed of 133MHz.



MICHAEL MUSTACCHI

Senior PowerPC architect Peter Sandon describes the L2 cache on IBM's new PowerPC 750CX.

On-Chip L2: New Package, Lower Cost

The new on-chip L2 cache is 256K in size and two-way set-associative. An L2 hit imposes an L1 miss penalty of five cycles, compared with eight cycles for the external L2 on the 750. The CX can transfer an entire 32-byte line into the L1 in four cycles, whereas the 750 requires eight cycles (with half-speed cache bus and commodity SRAMs). Assuming a 2%-per-instruction L1 miss rate and a 0.4%-per-instruction L2 miss rate, the 750CX should have a CPI (cycles per instruction) about 6.5% better than the 750. At the 10% higher frequency the CX will attain, performance should be about 15% higher overall.

On real code, of course, the performance boost will likely not be this large. IBM estimates that at 550MHz the CX will achieve a SPECint95 (base) score of 22.4 and a SPECfp95 (base) score of 13.3. This SPECint score indicates that the 750CX has about 5% better performance than a 750 with a 256K external L2 at the same clock rate, or about the same performance as a 750 with a 1M external L2 and a 10% lower frequency. Thus, since the CX operates at a 10% higher frequency than the 750, the CX essentially eliminates the cost of 1M of SRAM cache without sacrificing any performance.

In addition to eliminating the cost of 1M of SRAM, the 750CX die will also cost less to manufacture than the 750. The 750CX has a die size of only 42.7mm^2, almost the same size as its 40mm^2 predecessor. Even though the 0.18-micron CMOS-8S process used for the CX is currently a somewhat more expensive process than the more mature 0.22-micron copper CMOS-7S process used on the 750, the 750CX design eliminates the precision resistors required in the 750 design, thereby substantially lowering process costs. In addition, IBM improved the fault coverage in the CX design to more than 99% and shortened the internal scan chains for faster testing. Also, the physical design has been optimized with greater wire spacing to reduce shorts and with a larger number of redundant vias to reduce opens. The L2 includes ECC that can provide bit-line redundancy.

The most significant reduction in manufacturing cost, however, comes from the use of a new low-cost organic-laminate BGA package, shown in Figure 2. With this package, IBM breaks with its traditional C4-bonding technique (flip-chip), opting instead for old-fashioned wire-bond technology. This choice seems like a giant step backward for IBM: C4—a technology IBM pioneered—offers dramatically superior electrical characteristics. For that reason, the rest of the industry—even Intel—is rapidly converting to C4. Presumably, IBM opted for wire bonding on the CX because it is still slightly cheaper than C4.

With no need for a back-side cache bus, the new package requires only 256 I/O pads (139 of which are signals). A plastic substrate, wire bonding, and 25% fewer pads make the CX package considerably less costly than the 360-pad ceramic BGA used for the 750.

As with most previous PowerPC processors, power consumption of the CX is relatively low. At 550MHz and 1.8V, the 21.5-million-transistor part dissipates 9.3W worst case, but more typically it draws only about 4.6W. To help

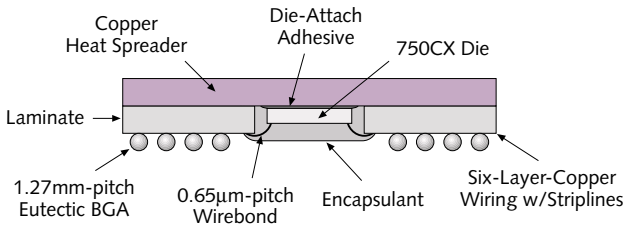


Figure 2. The new 256-pad organic-laminate BGA package uses wire bonding to reduce manufacturing costs to below those of IBM's traditional C4 (flip-chip) technique. An integrated copper heat spreader gives the package much lower thermal resistance (θ_{JC}) than conventional plastic packages.

dissipate this heat, the CX's package provides an integrated copper heat spreader, a feature that facilitates cooling with low-cost heat sinks.

Not PC Performance, But Lower Power and Cost

Although the 750CX won't bring PowerPC up to the performance of top-end 1GHz PC processors from Intel and AMD—which also have 256K on-chip L2s—the 750CX has significantly less than half the die size of those parts, and it consumes only a small fraction of their power. Intel's 1GHz Pentium III is 106mm^2 and typically burns about 23W; AMD's 1GHz Thunderbird is 120mm^2 and typically burns just shy of 50W.

Performancewise, the CX is more closely matched to Intel's and AMD's low-end desktop Celeron and Duron processors, both of which have L2s half the size of the CX's, but which operate at a 25% higher frequency. But once again, the CX has a much smaller die size and much lower power than these parts. The 700MHz Celeron is 106mm^2 and dissipates three times as much power as the CX; the 700MHz Duron is 100mm^2 and is roughly six times more power hungry (see *MPR 6/26/00-02*, "Duron Takes on Celeron") than the CX.

The CX is even somewhat more power stingy than Intel's latest 600/500MHz Mobile Coppermine in its battery-optimized (500MHz, 1.1V) SpeedStep mode (see *MPR 7/3/00-02*, "Intel Strikes Back at Transmeta"), a part the CX should handily outperform. The 750CX is also more than 40% smaller than both the 76mm^2 Cyrix III (see *MPR 6/26/00-03*, "Cyrix III is Dead, Long Live Cyrix III"), which has no on-chip L2, and Transmeta's 73mm^2 TM5400 VLIW Crusoe (see *MPR 2/14/00-01*, "Transmeta Breaks x86 Low-Power Barrier"), which is built in the same IBM process as the CX and has a 256K L2.

As embedded processors go, the 750CX is one of the highest-performance chips available. Of the processors that have officially reported EEMBC-benchmark scores (see *MDR 5/1/00-02*, "EEMBC Releases First Benchmarks"), the 750CX is by far the highest performer. The CX scored 8.7x faster than our reference chip (the NEC V832-143) on the EEMBC Telecom suite, 19.3x on the Automotive suite, and 8.5x on the Office Automation suite. No other part yet reported comes even close to these scores (see *www.eembc.org*).

With a Dhrystone 2.1 rating of 2.3 mips/MHz, a 550MHz 750CX should be slightly faster than the 2.0 mips/MHz MIPS R20K at 600MHz, a part that won't see first silicon until later this year (see *MPR 7/3/00-01*, "MIPS 20Kc Is Fastest Licensable Core"). Although the R20K is slightly smaller (34mm^2) than the CX in a 0.18-micron TSMC process, the R20K has the same size L1s and does not include any on-chip L2 cache. The CX may eventually take a performance backseat to the 2.0 mips/MHz SiByte SB-1, which is expected to run at up to 1GHz. But a chip based on that core isn't due until later in 2001 in a 0.15-micron process (see *MPR 6/26/00-04*, "SiByte Reveals 64-Bit Core for NPUs").

By that time, however, Sandon says IBM will have the 750CXe in production. This version will add no new features to the CX design, but it will boost frequency to 700MHz with an enhanced (CMOS-8SE) process that has more aggressive channel lengths (CX uses a relatively conservative L_{eff} of 0.097µm). At 700MHz, the CXe will deliver more than 1,600 mips and, with its on-chip L2, may give a 1GHz SB-1 a run for its money on real applications. While the R20K and the SB-1 are both 64-bit machines, whereas the CX is only 32 bits, it is unlikely that very many real-world embedded applications in 2001 will need the additional address space or ALU width.

At the least, the 750CX will provide a cost-effective upgrade for current PowerPC 750 customers. Apple, for one, should find the new part attractive for its low-end and portable boxes, although it needs to get on with its conversion to G4 processors and may not wish to get sidetracked with a short-term solution. The CX will provide, however, a very attractive upgrade for current 750 embedded customers. And, in the embedded market, the new chip is sufficiently compelling that it may even attract new customers into the PowerPC camp. ◇

Price & Availability

The PowerPC 750CX is sampling today at speeds ranging from 350MHz to 550MHz. A 400MHz part lists for $77 in quantities of 10,000 units; pricing for other speed grades were not announced. The faster 750CXe will sample in 4Q00. For more information check out IBM's Web site at *www.chips.ibm.com/products/powerpc/chips/750cx.html*.