THE INSIDER'S GUIDE TO MICROPROCESSOR HARDWARE

MOTO PAIRS STARCORE WITH MCORE FOR 3G

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At the recent Embedded Processor Forum, Motorola announced a new SoC architecture for implementing third-generation (3G) wireless terminal devices: the company will team a StarCore SC140 DSP core with Motorola's MCore architecture on a single chip. Motorola

did not announce a specific product, instead stating that it will customize the mixture of peripherals, memory, and I/O to match the needs of specific applications. The mixture may include customer-supplied IP as well as Motorola-designed IP blocks. At the Forum, Motorola acknowledged that the two cores alone are not sufficient for a complete 3G solution, and that SoC designers will have to add hardware coprocessors and accelerators to provide the needed additional performance. No other processor vendor has announced any processor (or two-processor combination, for that matter) capable of handling the demands of a full-blown 3G wireless appliance without additional hardware, so Motorola is not alone in this performance gap. Motorola expects to fabricate devices using 0.18-micron technology, with a migration path to 0.13 micron.

The particular variant of the MCore architecture that will be included in the SoC is the M340, which provides its own instruction/data cache and MMU. The M340 will execute at 100MHz. The SC140 DSP core will execute at 200MHz (significantly slower than the SC140's current top speed of 300MHz). Running interference between the two cores is an "Inter-Processor Communication Module" (IPCM), which is responsible for intercore data transfers and transfers between the cores and external memory. Motorola claims that the IPCM, which includes 32 channels of DMA and will execute at 100MHz, will alleviate data bandwidth bottlenecks and enable efficient memory sharing between the cores.

This is the second device Motorola has announced that includes an SC140; the MSC8101, announced in September

1999, includes a 300MHz SC140 and targets demanding line-powered applications such as cellular base stations. StarCore (the joint DSP development center of Lucent and Motorola) has claimed that the SC140 architecture is unusual in that it not only provides industry-leading performance but is the first high-performance DSP that is sufficiently energy-efficient to enable its use in portable devices (see MPR 5/10/99-03, "StarCore Reveals Its First DSP"). With Motorola's recent announcement, it appears that the company intends to fully capitalize on the core's unusual combination of strengths. This is probably the first time a single DSP core has targeted both the infrastructure equipment side and the portable side of a wireless application; using the same core for both may provide significant benefits in terms of code and knowledge-base reuse.

With this announcement, Motorola is challenging both ARM and Texas Instruments; ARM has the dominant MCU architecture in portable wireless devices, and TI claims that roughly 70% of wireless handsets contain TI DSPs (often on the same chip as an ARM). Obviously, Motorola is hoping to snag some of these two companies' market shares with its MCore/SC140 combination. Motorola has an unusual position in this market, in that it provides both processors for cell phones and the cell phones themselves. This situation may be an advantage, in the sense that Motorola may be inclined to use its own chips in its cell phones. It may also be a disadvantage, however, since, in some cases, Motorola will be competing with its own semiconductor customers.