PATENT WATCH

By Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send email to belgard@arithmetic.stanford.edu *with comments or questions.*

6,061,521

Computer having multimedia operations executable as two distinct sets of operations within a single instruction cycle

Filed: December 2, 1996 **Issued: May 9, 2000**
Inventors: John Thayer et al. **Claims: 11**
Assignee: Compaq

A multimedia extension unit (MEU) is provided for performing various multimedia operations. The MEU may be coupled, either through a coprocessor bus or a local CPU bus, to a conventional processor. In one embodiment, an arithmetic logic unit may be partitioned into at least two logic portions. A first logic portion may be coupled to receive a first operand from a fixed slot of a first register and a second operand from any slot of a second register. A second logic portion may be coupled to receive a third operand from a fixed slot of the first register and a fourth operand from any slot of the second register. The first logic portion may perform an arithmetic operation different from the second logic portion.

6,061,367

Processor with pipelining structure and method for high-speed calculation with pipelining processors

Filed: August 25, 1997 **Issued: May 9, 2000**
Inventor: Christian Siemers **Claims: 6**
Assignee: Siemens

A pipelined, superscalar processor includes a configurable logic unit and a multiplexer-controlled s-paradigm unit, linking contents of an integer register file to a functional unit with programmable structures and having a large number of data links connected by multiplexers. The s-paradigm unit has a programmable hardware structure for dynamic reconfiguration/programming while a program is running.

6,049,672

Microprocessor with circuits, systems, and methods for operating with patch micro-operation codes and patch microinstruction codes stored in multi-purpose memory structure

Filed: March 7, 1997 **Issued: April 11, 2000**
Inventors: Jonathan Shiell et al. **Claims: 20**
Assignee: TI

A microprocessor operates in response to microinstructions stored in a read-only memory. A microcode patch table, stored in data and/or macroinstruction caches, stores an indication of patch microinstructions. Each new microaddress is compared with the patch table entries. If there is no match, then a multiplexer selects the microinstruction recalled from within the microinstruction address read-only memory. If there is a match, then a corresponding patch microinstruction is recalled from the cache memory.

6,047,363

Prefetching data using profile of cache misses from earlier code executions

Filed: October 14, 1997 **Issued: April 4, 2000**
Inventor: Jurt Lewchuk **Claims: 20**
Assignee: AMD

During execution of a code sequence, a profile is generated containing addresses of the data cache misses experienced during the execution. The profile is associated with the code sequence such that, during a future execution of the code sequence, the profile is available. Prefetching may then be performed based on the profile.

6,044,222

System, method, and program product for loop instruction scheduling hardware lookahead

Filed: June 23, 1997 **Issued: March 28, 2000**
Inventor: Barbara Simons et al. **Claims: 21**
Assignee: IBM

Improved scheduling of instructions within a loop is provided for a computer system having hardware lookahead. A dependence graph is constructed which contains all the nodes of a dependence graph corresponding to the loop, but which only contains loop-independent dependence edges. Instructions may be scheduled for execution based on the dependence graph.

6,044,220

Method and apparatus for operating a data processor to execute software written using a foreign instruction set

Filed: February 25, 1997 **Issued: March 28, 2000**
Inventor: Mauricio Breternitz, Jr. **Claims: 9**
Assignee: Motorola

An instruction set interpreter and translator provides dynamic idiom recognition by use of a programmable hash table. Idioms are sequences of consecutive instructions that occur frequently during execution. Interpretive execution of such idioms is optimized to attain high performance. Idioms are recognized dynamically during interpretive execution. A programmable hash table is extended with entries corresponding to newly recognized idioms as their frequency of occurrence exceeds a threshold.