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BOPS Debuts Manta Silicon

By Peter N. Glaskowsky {8/7/00-03}

Some two and a half years after first describing its ManArray processor architecture at the Microprocessor Forum (see *MPR 10/27/97-msb*, "BOPS Raises Curtain on ManArray DSP"), BOPS has shown the first ManArray-based chip. In his presentation at the **Embedded Processor Forum** in June, David Baker, vice president of BOPS, described Manta, a chip with four DSP processing elements (PEs), each capable of 40 operations per clock at 125MHz. The combination delivers a peak throughput of 20 billion 8-bit integer operations and 3.2 billion floating-point operations per second, not counting the independent sequence processor (SP) that handles control and sequential functions.

PEs and SPs are tied together on Manta by a cluster switch (CS) that can connect together any two pairs of PEs (the SP is attached to one PE). Interprocessor transfers take place with just one cycle of latency. Four PEs with one SP and one CS constitute a cluster. Future chips will integrate multiple clusters with additional communication channels between CS units. Also part of Manta are a 32-bit, 66MHz PCI-bus interface; a 64-bit, 133MHz SDRAM controller; 128K of on-chip SRAM; and a MIPS-compatible 32-bit processor-bus interface. The chip is 169mm^2 in size, with 80mm^2 the core and the remainder SRAM.

BOPS will use the 412-pin, 4W Manta as a proof-of-concept vehicle for the ManArray architecture. The company stresses that Manta was designed using a standard ASIC design flow and is built in TSMC's mature 0.25-micron, five-layer-metal process. Although the chip is a good prototyping vehicle, BOPS expects customers to build application-specific chips in faster processes to achieve substantially higher performance.

Though the Manta PEs include both integer and floating-point execution units, PEs may also be built to support just one of these data types. BOPS offers nine configurations of the Manta core with fixed-point, floating-point, or both types of execution units in arrangements of from one to four processing elements. The company also offers a dual-issue floating-point core called Moray that is optimized for 3D-geometry processing and radio base-station applications. Each of these products is meant for use as a DSP coprocessor for MIPS and ARM host processors.

The first Manta chip is available in a PCI-bus evaluation board known as Jordan, which also includes a QED RM5231 MIPS-compatible processor and 64M of SDRAM. Although Manta is not available separately, the Jordan board is priced at $9,995 bundled with the BOPS software development kit. For more information, visit BOPS online at *www.bops.com*.