PATENT WATCH

By Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send email to belgard@arithmetic.stanford.edu *with comments or questions.*

6,067,601

Cache memory based instruction execution

Filed: November 3, 1997 **Issued: May 23, 2000**
Inventor: Donald Sollars **Claims: 49**
Assignee: Brecis Communications

A processor and methods using a cache-based approach to instruction execution. One or more control units operate a data cache to directly supply instruction operand values stored (and/or store result values) in the cache. The direct supplying and the direct accepting and storing are performed in response to the instructions, which specify the operands using logical addresses.

6,065,115

Processor and method for speculatively executing instructions from multiple instruction streams indicated by a branch instruction

Filed: April 10, 1998 **Issued: May 16, 2000**
Inventors: Harshvardhan Sharangpani et al. **Claims: 31**
Assignee: Intel

A microprocessor with conditional branch instructions. A fetch unit fetches instructions and branch prediction logic, coupled to the fetch unit, and predicts conditional branch conditions. The branch prediction logic also determines whether resolution of the condition is unlikely to be predicted accurately. Stream management logic responsive to the branch prediction logic directs speculative processing of instructions from both code sections, prior to resolution of the condition if resolution of the condition is unlikely to be predicted accurately.

6,065,103

Speculative store buffer

Filed: December 16, 1997 **Issued: May 16, 2000**
Inventors: Thang Tran et al. **Claims: 18**
Assignee: AMD

A speculative store buffer is updated by speculative store memory operations. Instead of performing dependency checking for load operations among the operations buffered in a load/store unit, the load/store unit performs a lookup in the speculative store buffer. If a hit is (or hits are) detected in the speculative store buffer, the most recent result is forwarded to the load. Since dependency checking against the memory operation buffers is not performed, the dependency checking limitations as to the size of these buffers may be eliminated.

6,065,091

Translation look-aside buffer slice circuit and method of operation

Filed: May 30, 1997 **Issue: May 16, 2000**
Inventor: Daniel Green **Claims: 40**
Assignee: VIA-Cyrix

A look-aside slice supporting a primary TLB for use in a processor with a physically addressed cache. The TLB-slice contains a copy of some of the address bits of the physical addresses that the primary TLB contains in its mapping of logical to physical addresses. The TLB-slice is located physically closer to the cache than the primary TLB, allowing pre-select signals to be sent to the cache.

6,065,027

Data processor with up pointer walk trie [sic] *traversal instruction set extension*

Filed: November 9, 1998 **Issued: May 16, 2000**
Inventors: John Cashman et al. **Claims: 11**
Assignee: Cisco Technology

A programmable communications processor device including a "partial compare and conditional move" instruction. The instruction can be used for protocols requiring decompression or decryption of data. The instruction is defined to perform a comparison between the first and second input data. If they are equal, then a terminate state is set; otherwise, the first input data is copied to a predefined location and no state is set. The instruction may be used for trie traversals.

6,044,456

Electronic system and method for maintaining synchronization of multiple front-end pipelines

Filed: January 5, 1998 **Issued: March 28, 2000**
Inventors: Keshavram Murty et al. **Claims: 25**
Assignee: Intel

A system and method for maintaining synchronization of multiple front-end pipelines operating in parallel. The multiple front-end pipelines perform their own operations, but on the same instruction. These multiple front-end pipelines can become asynchronous to each other in response to a stall condition: for example, a TLB or cache miss. On a stall, the pipelines are flushed and then reloaded. Upon release of the stall condition, the pipelines are released at different periods of time, such that later in the flow the pipelines will become resynchronized.

OTHER ISSUED PATENTS

6,065,112 *Microprocessor with arithmetic processing units and arithmetic execution unit*

6,065,110 *Method and apparatus for loading an instruction buffer of a processor capable of out-of-order instruction issue*