Bt477

Advance Information

This document contains information on a product under development. The parametric information are target parameters and are subject to change.

80 MHz 256 Word Color Palette Personal System/2® Power-Down RAMDAC™

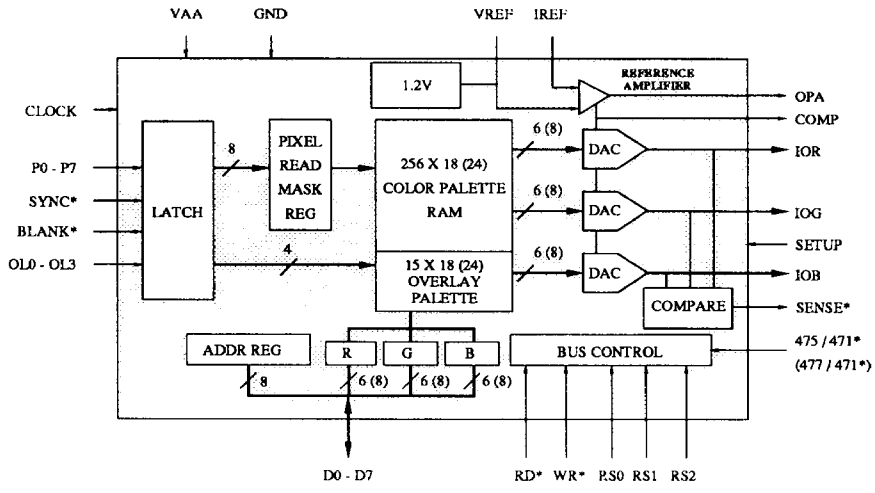
Distinguishing Features

- 80, 66, 50, 35 MHz Operation
- Bt471/476/478 Pin Compatible
- Power-Down Mode
- Anti-Sparkle Circuitry
- Analog Output Comparators
- Triple 6-bit (8-bit) D/A Converters
- 256 x 18 (24) Color Palette RAM
- RS-343A/RS-170 Compatible Outputs
- 15 x 18 (24) Overlay Registers
- Programmable Pedestal
- Optional Internal Reference
- 44-pin PLCC Package

Applications

- High Resolution Color Graphics
- CAE/CAD/CAM Applications
- Image Processing
- Instrumentation
- Desktop Publishing

Functional Block Diagram



Product Description

The Bt475 and Bt477 RAMDACs are designed specifically for Personal System/2® compatible color graphics.

The Bt475 has a 256 x 18 lookup table RAM, 15 x 18 overlay registers, and triple 6-bit D/A converters.

The Bt477 has a 256 x 24 lookup table RAM, 15 x 24 overlay registers, and triple 8-bit D/A converters. Both 6-bit and 8-bit color modes are supported.

On-chip analog output comparators are included to simplify diagnostics and debugging, with the result output onto the SENSE* pin. Also included is an on-chip voltage reference to simplify using the device.

A power-down mode is available to reduce power requirements when the analog outputs are not used. This is useful in laptop computer systems that need the option of driving an external RGB monitor.

When the 475/471* input pin (477/471* on the Bt477) is floating or a logical zero, the Bt475 and Bt477 behave exactly as a Bt471 with anti-sparkle capabilities, on-chip reference, and analog comparators. When the pin is a logical one, the additional capabilities of the command register are available.

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Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt475/477 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers.

The RS0 - RS2 select inputs specify whether the MPU is accessing the address register, color palette RAM, overlay registers, or read mask register, as shown in Table 1. The 8-bit address register is used to address the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

Writing Color Palette RAM Data

To write color data, the MPU writes the address register (RAM write mode) with the address of the color palette RAM location to be modified. The MPU performs three successive write cycles (6 or 8 bits each of red, green, and blue), using RS0 - RS2 to select the color palette RAM. After the blue write cycle, the three bytes of color information are concatenated into a 18-bit or 24-bit word and written to the location specified by the address register. The address register then increments to the next location which the MPU may modify by simply writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R,G,B write cycles until the entire block has been written.

Reading Color Palette RAM Data

To read color palette RAM data, the MPU loads the address register (RAM read mode) with the address of the color palette RAM location to be read. The contents of the color palette RAM at the specified address are copied into the RGB registers and the address register is incremented to the next RAM location. The MPU performs three successive read cycles (6 or 8 bits each of red, green, and blue), using RS0 - RS2 to select the color palette RAM. Following the blue read cycle, the contents of the color palette RAM at the address specified by the address register are copied into the RGB registers and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R,G,B read cycles until the entire block has been read.

Writing Overlay Color Data

To write overlay color data, the MPU writes the address register (overlay write mode) with the address of the overlay location to be modified. The MPU performs three successive write cycles (6 or 8 bits each of red, green, and blue), using RS0 - RS2 to select the overlay registers. After the blue write cycle, the three bytes of color information are concatenated into a 18-bit or 24-bit word and written to the overlay location specified by the address register. The address register then increments to the next location which the MPU may modify by simply writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R,G,B write cycles until the entire block has been written.

RS2	RS1	RS0	Addressed by MPU
0	0	0	address register (RAM write mode)
0	1	1	address register (RAM read mode)
0	0	1	color palette RAM
0	1	0	pixel read mask register
1	0	0	address register (overlay write mode)
1	1	1	address register (overlay read mode)
1	0	1	overlay registers
1	1	0	command register

Table 1. Control Input Truth Table.

Circuit Description (continued)

Reading Overlay Color Data

To read overlay color data, the MPU loads the address register (overlay read mode) with the address of the overlay location to be read. The contents of the overlay register at the specified address are copied into the RGB registers and the address register is incremented to the next overlay location. The MPU performs three successive read cycles (6 or 8 bits each of red, green, and blue), using RS0 - RS2 to select the overlay registers. Following the blue read cycle, the contents of the overlay location at the address specified by the address register are copied into the RGB registers and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R,G,B read cycles until the entire block has been read.

Additional Information

When accessing the color palette RAM, the address register resets to $00 following a blue read or write cycle to RAM location $FF. While accessing the overlay color registers, the four most significant bits of the address register (ADDR4 - 7) are ignored.

The MPU interface operates asynchronously to the pixel clock. Data transfers between the color palette RAM/overlay registers and the color registers (R, G, and B in the block diagram) are synchronized by internal logic, and occur in the period between MPU accesses. To reduce noticable sparkling on the CRT screen during MPU access to the color palette RAMs, internal logic maintains the previous output color data on the analog outputs while the transfer between lookup table RAMs and the RGB registers occurs.

To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table 2. They are reset to zero when the MPU writes to the address register, and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other eight bits of the address register, incremented following a blue read or write cycle, (ADDR0 - 7) are accessible to the MPU, and are used to address color palette RAM locations and overlay registers, as shown in Table 2. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

Note the pixel clock must be active for MPU accesses to the color palette RAM.

Bt471 Compatible Operation

If the 475/471* (477/471*) pin is a logical zero, the Bt475/477 operates as a Bt471 RAMDAC; the command register is disabled and 6-bit operation is selected. Color data is contained on the lower six bits of the data bus, with D0 being the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be a logical zero. Note that in the 6-bit mode, the Bt477's full scale output current will be about 1.5% lower than when in the 8-bit mode. This is due to the 2 LSBs of each 8-bit DAC always being a logical zero in the 6-bit mode.

If the 475/471* (477/471*) input is a logical one, the command register is available. On the Bt477, the 6-bit/8-bit select bit in the command register may be used to specify whether 6-bit or 8-bit color data values are being used

	Value	RS2	RS1	RS0	Addressed by MPU
ADDRa, b (counts modulo 3)	00 01 10				red value green value blue value
ADDR0 - 7 (counts binary)	$00 - $FF xxxx 0000 xxxx 0001 : xxxx 1111	0 1 1 : 1	0 0 0 : 0	1 1 1 : 1	color palette RAM reserved overlay color 1 : overlay color 15

Table 2. Address Register (ADDR) Operation.

Circuit Description (continued)

8-bit / 6-bit Color Selection

For 8-bit operation, D0 is the LSB and D7 is the MSB of color data.

For 6-bit operation, color data is contained on the lower six bits of the data bus, with D0 being the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be a logical zero.

Note that in the 6-bit mode, the Bt477's full scale output current will be about 1.5% lower than when in the 8-bit mode. This is due to the 2 LSBs of each 8-bit DAC always being a logical zero in the 6-bit mode.

Power Down Mode

The Bt475/477 incorporates a power-down capability, controlled by the SLEEP command bit. While the SLEEP bit is a logical zero, the Bt475/477 functions normally.

While the SLEEP bit is a logical one, the DACs and power to the RAM is turned off. Note that the RAM still retains the data. Also, the RAM may still be read or written to while sleeping as long as the pixel clock is running. The RAM automatically powers-up during MPU read/write cycles, and shuts down when the MPU access is completed.

The DACs will be turned off during sleep mode only if a voltage reference (internal or external) is used. If using an external current reference, external circuitry should turn the current reference off during sleep mode.

SENSE Output*

SENSE* is a logical zero if one or more of the IOR, IOG, and IOB outputs have exceeded the internal voltage reference level (335 mV). This output is used to determine the presence of a CRT monitor and via diagnostic code, the difference between a loaded or unloaded RGB line can be discerned. The 335 mV reference has a ± 5% tolerance (when using an external 1.235v voltage reference). The tolerance is ± 10% when using the internal voltage reference or an external current reference. Note that SYNC* should be a logical zero for SENSE* to be stable.

Frame Buffer Interface

The P0 - P7 and OL0 - OL3 inputs are used to address the color palette RAM and overlay registers, as shown in Table 3. The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bit-wise logically ANDed with the P0 - P7 inputs. Bit D0 of the pixel read mask register corresponds to pixel input P0. The addressed location provides 18 bits (Bt475) or 24 bits (Bt477) of color information to the three D/A converters.

The SYNC* and BLANK* inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 1 and 2. Tables 4 and 5 detail how the SYNC* and BLANK* inputs modify the output levels.

The SETUP input pin is logically ANDed with the SETUP command bit and is used to specify whether a 0 or 7.5 IRE blanking pedestal is to be used.

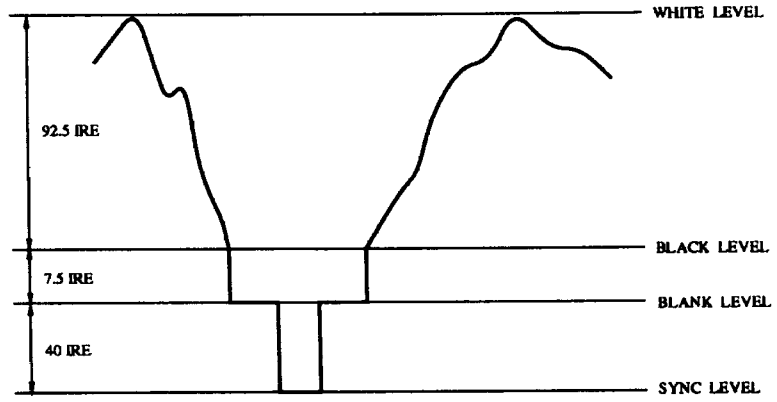
The analog outputs of the Bt475/477 are capable of directly driving a 37.5-ohm load, such as a doubly-terminated 75-ohm coaxial cable.

OL0 - OL3	P0 - P7	Addressed by frame buffer
$0	$00	color palette RAM location $00
$0	$01	color palette RAM location $01
:	:	:
$0	$FF	color palette RAM location $FF
$1	$xx	overlay color 1
:	$xx	:
$F	$xx	overlay color 15

Table 3. Pixel and Overlay Control Truth Table. (Pixel Read Mask Register = $FF)

Circuit Description (continued)

NO SYNC		SYNC	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75-ohm doubly-terminated load, SETUP = 7.5 IRE. VREF = 1.235v, RSET = 147 ohms. RS-343A levels and tolerances assumed on all levels.

Figure 1. RS-343A Composite Video Output Waveforms. (SETUP = 7.5 IRE)

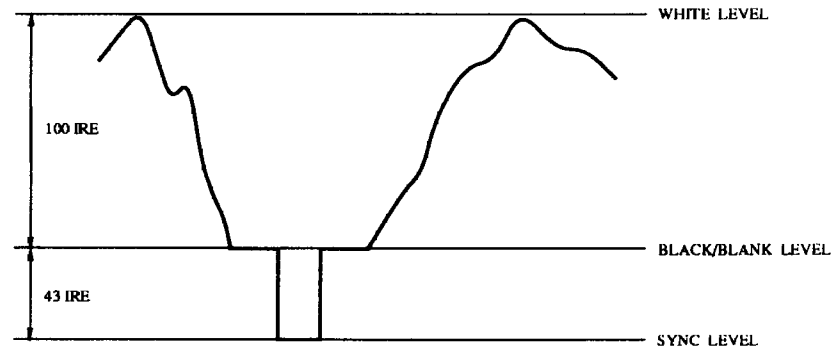
Description	Sync Disabled	Sync Enabled	SYNC*	BLANK*	DAC Input Data
	Iout (mA)	Iout (mA)			
WHITE	19.05	26.67	1	1	$FF
DATA	data + 1.44	data + 9.05	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	1.44	9.05	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	0	7.62	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 75-ohm doubly-terminated load, SETUP = 7.5 IRE. VREF = 1.235v, RSET = 147 ohms.

Table 4. RS-343A Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description (continued)

NO SYNC		SYNC	
MA	V	MA	V
17.62	0.660	25.24	0.950
0.00	0.000	7.62	0.286
0.00	0.000	0.00	0.000



Note: 75-ohm doubly-terminated load, SETUP = 0 IRE. VREF = 1.235v, RSET = 147 ohms. RS-343A levels and tolerances assumed on all levels.

Figure 2. RS-343A Composite Video Output Waveforms. (SETUP = 0 IRE)

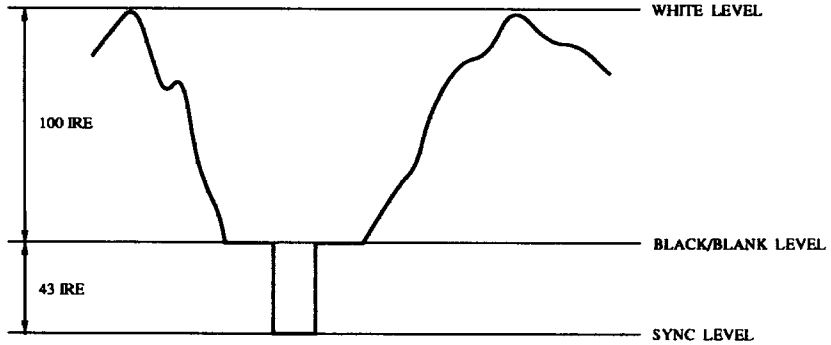
Description	Sync Disabled	Sync Enabled	SYNC*	BLANK*	DAC Input Data
	Iout (mA)	Iout (mA)			
WHITE	17.62	25.24	1	1	$FF
DATA	data	data + 7.62	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	0	7.62	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	0	7.62	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 75-ohm doubly-terminated load, SETUP = 0 IRE. VREF = 1.235v, RSET = 147 ohms.

Table 5. RS-343A Video Output Truth Table (SETUP = 0 IRE).

Circuit Description (continued)

NO SYNC		SYNC	
MA	V	MA	V
14.25	0.713	20.36	1.018
0.00	0.000	6.11	0.305
0.00	0.000	0.00	0.000



Note: 50-ohm load, SETUP = 0 IRE. VREF = 1.235v, RSET = 182 ohms. PS/2 levels and tolerances assumed on all levels.

Figure 3. PS/2 Composite Video Output Waveforms. (SETUP = 0 IRE)

Description	Sync Disabled	Sync Enabled	SYNC*	BLANK*	DAC Input Data
	Iout (mA)	Iout (mA)			
WHITE	14.25	20.36	1	1	$FF
DATA	data	data + 6.11	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	0	6.11	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	0	6.11	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 50-ohm load, SETUP = 0 IRE. VREF = 1.235v, RSET = 182 ohms.

Table 6. PS/2 Video Output Truth Table (SETUP = 0 IRE).

Internal Registers

Command Register

This register is operational only while the 475/471* (477/471*) pin is a logical one. It may be written to or read by the MPU at any time and is not initialized.

D7	reserved (logical zero)	A logical zero must be written to this bit when writing to the command register to ensure proper operation.
D6	Clock inhibit (0) normal operation (1) inhibit clocking	A logical one inhibits the internal clocking of the Bt475/477 to further reduce power during sleep mode. The command register may still be accessed at any time; however, the lookup table RAM may not be accessed by the MPU while the clock is inhibited. The integrity of the lookup table RAM is not guaranteed while the clock is inhibited.
D5	SETUP select (0) 0 IRE (1) 7.5 IRE	This bit specifies the blanking pedestal to be either 0 or 7.5 IRE. this bit is logically ANDed with the SETUP input pin; thus, if the SETUP input pin is a logical zero, this bit will be a logical zero.
D4	Blue sync enable (0) no sync on blue (1) sync on blue	This bit specifies whether the IOB output is to contain sync information or not.
D3	Green sync enable (0) no sync on green (1) sync on green	This bit specifies whether the IOG output is to contain sync information or not.
D2	Red sync enable (0) no sync on red (1) sync on red	This bit specifies whether the IOR output is to contain sync information or not.

Internal Registers (continued)

Command Register (continued)

D1	6-bit / 8-bit select (0) 6-bit (1) 8-bit	On the Bt477, this bit specifies whether the MPU is reading and writing 8 bits (logical one) or 6 bits (logical zero) of color information each cycle. The value of this bit is ignored on the Bt475.
D0	SLEEP enable (0) normal operation (1) sleep mode	While this bit is a logical zero, the Bt475/477 functions normally. If this bit is a logical one, the DACs and power to the RAM is turned off. Note that the RAM still retains the data. Also, the RAM may be read or written to as long as the pixel clock is running. The RAM automatically powers-up during MPU read/write cycles, and shuts down when the MPU access is completed. It requires about 1 second for the Bt475/477 to output valid video data after enabling normal operation (coming out of sleep mode). The DACs will be turned off during sleep mode only if a voltage reference (internal or external) is used. If using an external current reference, external circuitry should turn the current reference off during sleep mode.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level, as illustrated in Tables 4, 5 and 6. It is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SETUP	Setup control input (TTL compatible). Used to specify either a 0 IRE (logical zero) or 7.5 IRE (logical one) blanking pedestal. This pin should not be left floating.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the analog outputs (see Figures 1, 2, and 3). SYNC* does not override any other control or data input, as shown in Tables 4, 5, and 6; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK. If sync information is not required on the video outputs, SYNC* should be connected to GND.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the P0 - P7, OL0 - OL3, SYNC*, and BLANK* inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK by driven by a dedicated TTL buffer to avoid reflection-induced jitter.
P0 - P7	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. They are latched on the rising edge of CLOCK. P0 is the LSB. Unused inputs should be connected to GND.
OL0 - OL3	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information, as illustrated in Table 3. When accessing the overlay palette, the P0 - P7 inputs are ignored. They are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
COMP	Compensation pin. If an external or the internal voltage reference is used (Figures 4 and 5), this pin should be connected to OPA. If an external current reference is used (Figure 6), this pin should be connected to IREF. A 0.1 µF ceramic capacitor must always be used to bypass this pin to VAA. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
VREF	Voltage reference input. If an external voltage reference is used (Figure 5), it must supply this input with a 1.2v (typical) reference. If an external current reference is used (Figure 6), this pin should be left floating, except for the bypass capacitor. A 0.1 µF ceramic capacitor must always be used to decouple this input to VAA, as shown in Figures 4, 5, and 6. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. When using the internal reference, this pin should not drive any external circuitry, except for the decoupling capacitor (Figure 4).
OPA	Reference amplifier output. If an external or the internal voltage reference is used (Figures 4 and 5), this pin must be connected to COMP. When using an external current reference (Figure 6), this pin should be left floating.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly-terminated 75-ohm coaxial cable (Figures 4, 5, and 6).
VAA	Analog power. All VAA pins must be connected.
GND	Analog ground. All GND pins must be connected.

Pin Descriptions (continued)

Pin Name **Description**

Full scale adjust control. Note that the IRE relationships in Figures 1, 2, and 3 are maintained, regardless of the full scale output current.

When using an external or the internal voltage reference (Figures 4 and 5), a resistor (RSET) connected between this pin and GND controls the magnitude of the full scale video signal. The relationship between RSET and the full scale output current on each output is:

$$RSET\ (ohms) = K * 1{,}000 * VREF\ (v) / Iout\ (mA)$$

K is defined in the table below. It is recommended that a 147-ohm RSET resistor be used for doubly-terminated 75-ohm loads (i.e. RS-343A applications). For PS/2 applications (i.e. 0.7v into 50 ohms with no sync), a 182-ohm RSET resistor is recommended.

When using an external current reference (Figure 6), the relationship between IREF and the full scale output current on each output is:

$$IREF\ (mA) = Iout\ (mA) / K$$

Part	Mode	Pedestal	K (with sync)	K (no sync)
Bt477	6-bit	7.5 IRE	3.170	2.26
	8-bit	7.5 IRE	3.195	2.28
	6-bit	0 IRE	3.000	2.10
	8-bit	0 IRE	3.025	2.12
Bt475	(6-bit)	7.5 IRE	3.170	2.26
		0 IRE	3.000	2.10

WR* — Write control input (TTL compatible). D0 - D7 data is latched on the rising edge of WR*, and RS0 - RS2 are latched on the falling edge of WR* during MPU write operations. RD* and WR* should not be asserted simultaneously.

RD* — Read control input (TTL compatible). To read data from the device, RD* must be a logical zero. RS0 - RS2 are latched on the falling edge of RD* during MPU read operations. RD* and WR* should not be asserted simultaneously.

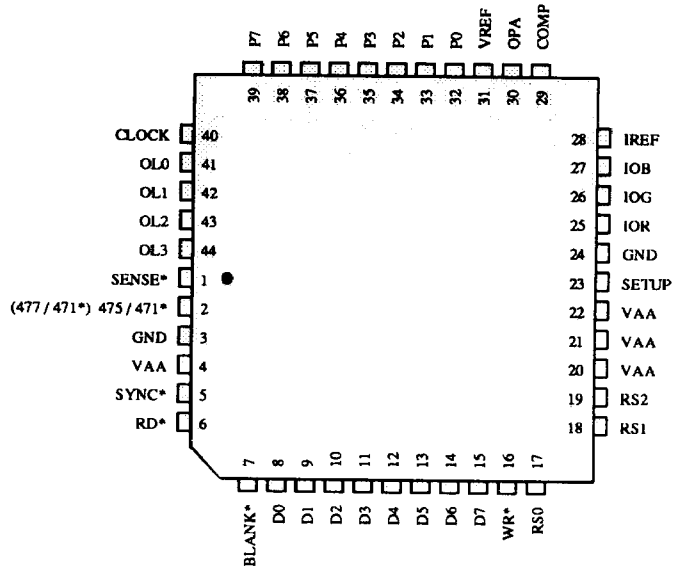
RS0, RS1, RS2 — Register select inputs (TTL compatible). RS0 - RS2 specify the type of read or write operation being performed, as illustrated in Tables 1 and 2.

D0 - D7 — Data bus (TTL compatible). Data is transferred into and out of the device over this eight bit bidirectional data bus. D0 is the least significant bit.

475/471* (477/471*) — Bt475 (Bt477) or B471 select input (TTL compatible). When the 475/471* (477/471*) input pin is floating or a logical zero, the Bt475/477 behaves exactly as a Bt471 with anti-sparkle capabilities. When the 475/471* (477/471*) input pin is a logical one, the extra capabilities of the Bt475/477 command register are available.

SENSE* — Sense output (TTL compatible). SENSE* is a logical zero if one or more of the IOR, IOG, and IOB outputs have exceeded the internal voltage reference level (335 mV). Note that SENSE* may not be stable while SYNC* is toggling.

Pin Descriptions (continued)



Names in parentheses are pin names for the Bt477.

PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt475/477 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of VAA and GND pins should be minimized so as to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. Ground planes must provide a low-impedance return path for the digital circuits. A 4-layer PC board is recommended with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for power and ground.

The optimum layout enables the Bt475/477 to be located as close to the power supply connector and as close to the video output connector as possible.

Ground Planes

For optimum performance, a common digital and analog ground plane with tub isolation (at least an 1/8" gap) and connected together only at the power supply connector (or the lowest impedance source) is recommended. Ground plane partitioning should extend the analog ground plane no more than 2" from the power supply connector to preserve digital noise margins during MPU read cycles. Thus, the ground tub isolation technique is constrained by the noise margin degradation during digital readback of the Bt475/477.

The digital ground plane should be under all digital signal traces to minimize radiated noise and crosstalk.

The analog ground plane should include all Bt475/477 ground pins, all reference circuitry and decoupling (external reference if used, RSET resistors, etc.), power supply bypass circuitry for the Bt475/477, analog output traces, COMP decoupling, and the video output connector.

Alternately, acceptable performance can usually be obtained by using a single common ground plane for the digital circuitry and the Bt475/477.

Unless the tub isolation technique is correctly implemented, it will result in worse performance than using a single, common ground plane.

Power Planes

A separate digital and analog power plane is necessary. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt475/477 power pins, any reference circuitry, and COMP and reference decoupling. There should be at least an 1/8" gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figures 4, 5, and 6. This bead should be located within three inches of the Bt475/477 and provides resistance to switching currents, acting as a resistance at high frequencies. A low resistance bead should be used, such as Ferroxcube VK20019-4B, Fair-Rite 2743001111, or Philips 431202036690.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the digital power and ground planes do not overlay portions of the analog power and ground planes, unless they can be arranged such that the plane-to-plane noise is common mode.

Device Decoupling

For optimum performance, all capacitors should be located as close to the device as possible, using the shortest leads possible (consistent with reliable operation) to reduce the lead inductance. Although chip capacitors have minimum inductance, radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

Best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor decoupling each of the two groups of VAA pins to GND. For operation above 75 MHz, a 0.1 µF capacitor in parallel with a 0.001 µF chip capacitor is recommended. The capacitors should be placed as close as possible to the device.

The 10 µF capacitor is for low frequency power supply supply ripple; the 0.1 µF capacitors are for high frequency power supply noise rejection.

PC Board Layout Considerations (continued)

A linear regulator to provide the analog power supply is recommended if the power supply noise is ≥ 200 mV or greater than 10 LSBs. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that power supply hum and ripple noise less than 1 MHz will couple about 10% of the noise onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically using a 0.1 µF ceramic capacitor. Low frequency supply noise will require a larger value. Lead lengths should be minimized for best performance.

If the display has a "ghosting" problem, additional capacitance in parallel with the COMP capacitor may help fix the problem.

Digital Signal Interconnect

The digital inputs to the Bt475/477 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and ground planes.

Most noise on the analog outputs will be caused by excessive edge speeds, overshoot, undershoot, and ringing on the digital inputs.

The digital edge speeds should be no faster than necessary, as feedthrough noise is proportional to the digital edge speeds. Lower speed applications will benefit using lower speed logic (3 - 5 ns edge rates) to reduce data-related noise on the analog outputs.

Digital interconnect distances for logic driving the Bt475/477 should be kept as short as possible (preferably less than 3 inches). Transmission line mismatch will exist if the line length reflection time is greater than 1/4 the signal edge time, resulting in ringing, overshoot, and undershoot that can generate noise onto the analog outputs. Line termination or reducing the line length is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ringing may be controlled by damping the line with a series resistor (10 to 50 ohms).

Long clock lines to the Bt475/477 should be avoided since this is another source of noise pickup.

Radiation of digital signals can also be picked up by the analog circuitry. Prevention is done by reducing the digital edge speeds (rise/fall time), minimizing ringing by using damping resistors, and minimizing coupling through PC board capacitance by routing 90 degrees to any analog signals.

Ensure that the power pins for the clock driver are properly decoupled to minimize transients. Minimize edge speeds and ringing, using damping resistors (10 to 50 ohms) or parallel termination where necessary.

If using parallel termination on digital signals, the resistors should be connected to the digital power and ground planes, not the analog power and ground planes.

Analog Signal Interconnect

The Bt475/477 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

For maximum performance, the analog outputs should have a source load resistor equal to the destination termination (via a clean isolated ground return path). The load resistor connection between the current output and GND should be as close as possible to the Bt475/477 to minimize reflections. Unused analog outputs should be connected to GND.

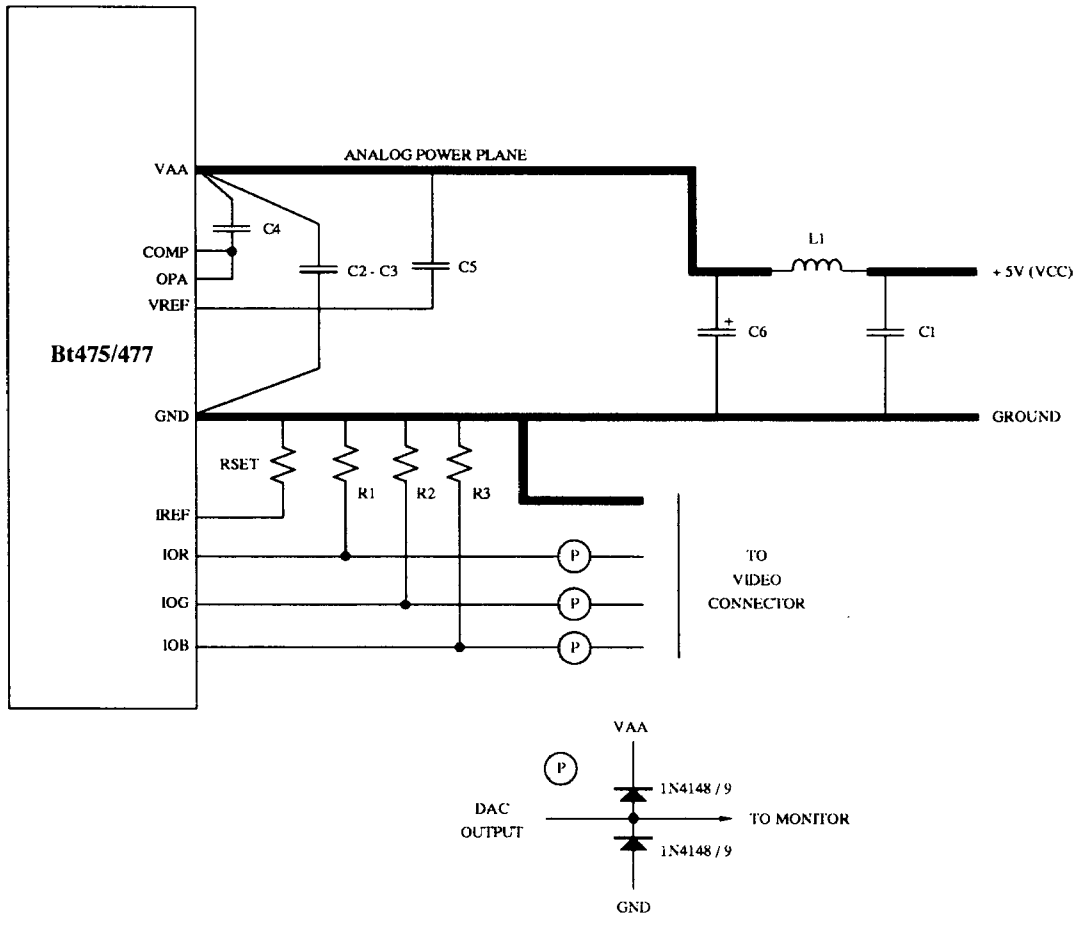
Analog edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, benefiting EMI and noise reduction.

Analog Output Protection

The B475/477 analog outputs should be protected against high energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figures 4, 5, and 6 can prevent latch-up under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 are low capacitance, fast switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations (continued)

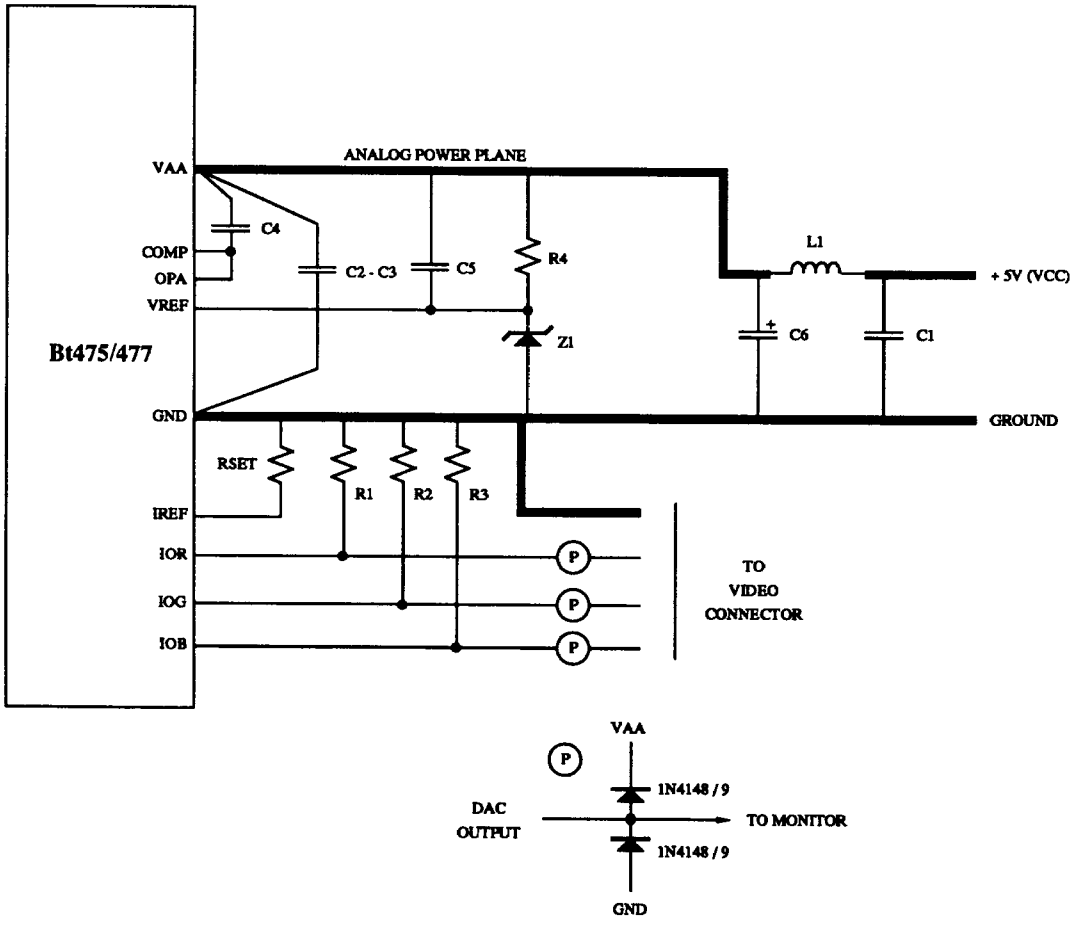


Location	Description	Vendor Part Number
C1 - C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75-ohm 1% metal film resistor	Dale CMF-55C
RSET	1% metal film resistor	Dale CMF-55C

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt475/477.

Figure 4. Typical Connection Diagram and Parts List. (Internal Voltage Reference)

PC Board Layout Considerations (continued)

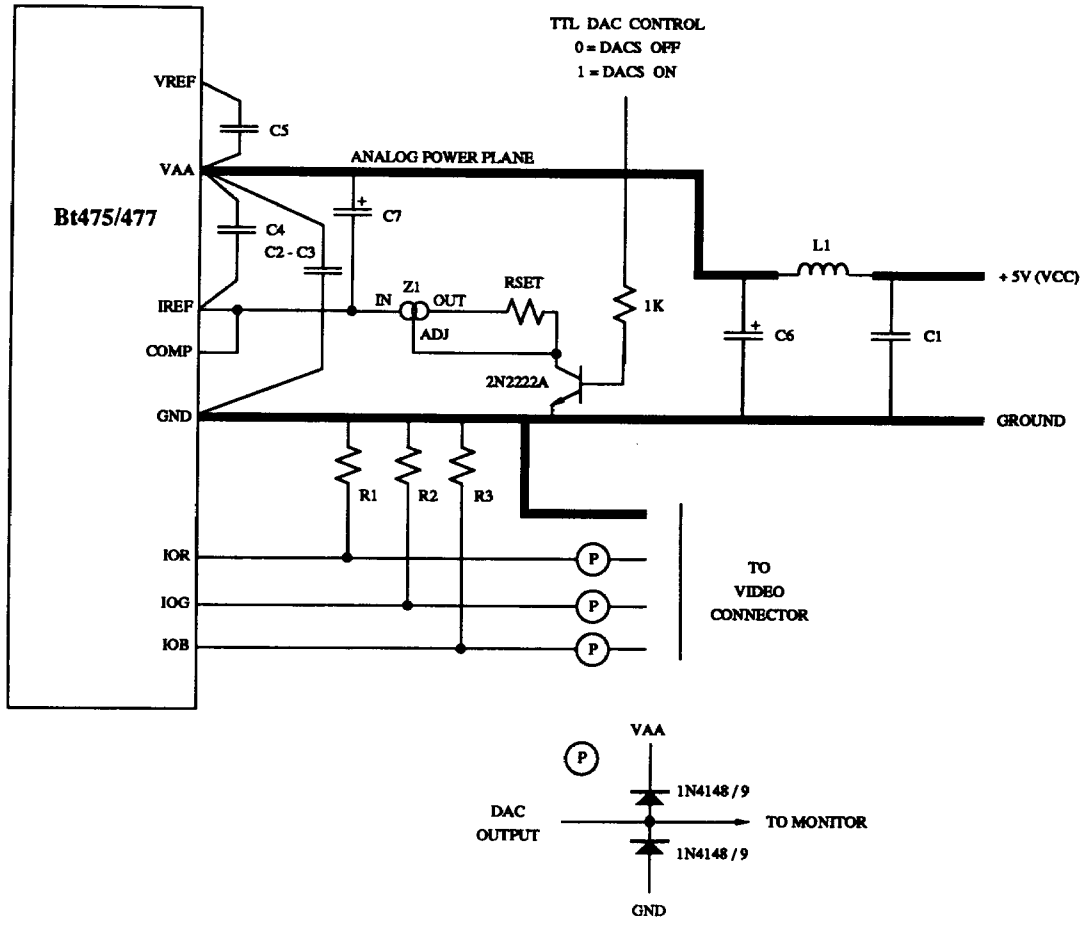


Location	Description	Vendor Part Number
C1 - C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75-ohm 1% metal film resistor	Dale CMF-55C
R4	1k-ohm 5% resistor	
RSET	1% metal film resistor	Dale CMF-55C
Z1	1.2v voltage reference	National Semiconductor LM385BZ-1.2

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt475/477.

Figure 5. Typical Connection Diagram and Parts List. (External Voltage Reference)

PC Board Layout Considerations (continued)



Location	Description	Vendor Part Number
C1 - C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
C7, C8	1 µF capacitor	Mallory CSR13G105KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75-ohm 1% metal film resistor	Dale CMF-55C
Z1	adjustable regulator	National Semiconductor LM317LZ
RSET	1% metal film resistor	Dale CMF-55C

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt475/477.

Figure 6. Typical Connection Diagram and Parts List. (External Current Reference)

Application Information

Using Multiple Devices

When using multiple Bt475/477s, each Bt475/477 should have its own power plane ferrite bead. If using the internal reference, each Bt475/477 should use its own internal reference.

Although the multiple Bt475/477s may be driven by a common external voltage/current reference, higher performance may be obtained if each RAMDAC uses its own reference. This will reduce the amount of color channel crosstalk and color palette interaction.

Each Bt475/477 must still have its own individual RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and reference capacitors.

Reference Selection

An external voltage reference provides about 10x better power supply rejection on the analog outputs than an external current reference.

Sleep Operation

When using the internal or external voltage reference, the DACs will be turned off during sleep mode.

When using an external voltage reference, some internal circuitry will still be powered during the sleep mode, resulting in 0.5 mA of power supply current being drawn (above the rated supply current specifications). This unnecessary current drain can be disabled by turning off the external voltage reference during sleep mode. As shown in Figure 4, a TTL signal and the 2N2222 transistor are used to disable the voltage reference during sleep mode. If the additional 0.5 mA current drain is acceptable, the 1K resistor and 2N2222 transistor are not required.

When using an external current reference, the DACs are not turned off during the sleep mode. To disable the DACs during sleep mode, the current reference must be turned off. As shown in Figure 5, a TTL signal and the 2N2222 transistor are used to disable the current reference during sleep mode.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA				
80, 66 MHz Parts		4.75	5.00	5.25	Volts
50, 35 MHz Parts		4.5	5.00	5.5	Volts
Ambient Operating Temperature	TA	0		+ 70	°C.
Output Load	RL		37.5		Ohms
Voltage Reference Configuration					
Reference Voltage	VREF	1.14	1.235	1.26	Volts
Current Reference Configuration					
IREF Current	IREF				
Standard RS-343A		- 3	- 8.39	- 10	mA
PS/2 Compatible		- 3	- 8.88	- 10	mA

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	Volts
Voltage on any Digital Pin		GND - 0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ			+ 150	°C.
Vapor Phase Soldering (1 minute)	TVSOL			220	°C.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)					
Bt475		6	6	6	Bits
Bt477		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL				
Bt475				± 1/4	LSB
Bt477				± 1	LSB
Differential Linearity Error	DL				
Bt475				± 1/4	LSB
Bt477				± 1	LSB
Gray Scale Error				± 5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	GND - 0.5		0.8	Volts
Input High Current (Vin = 2.4v)	IIH			1	µA
Input Low Current (Vin = 0.4v)	IIL			- 1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4v)	CIN			7	pF
Digital Outputs					
Output High Voltage (IOH = -400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	Volts
3-State Current	IOZ			50	µA
Output Capacitance	CDOUT			7	pF

See test conditions on next page.

D.C. Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Gray Scale Current Range				20	mA
Output Current					
White Level Relative to Black*		15.86	17.62	19.40	mA
Black Level Relative to Blank					
Setup = 7.5 IRE		0.95	1.44	1.90	mA
Setup = 0 IRE		0	5	50	µA
Blank Level					
Sync Enabled		6.29	7.62	8.96	mA
Sync Disabled		0	5	50	µA
Sync Level		0	5	50	µA
LSB Size					
Bt475			279.68		µA
Bt477			69.1		µA
DAC to DAC Matching			2	5	%
Output Compliance	VOC	- 1.0		+ 1.5	Volts
Output Impedance	RAOUT		10		K ohms
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT			30	pF
Voltage Reference Input Current	IVREF		10		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 KHz)	PSRR			0.5	% / % ΔVAA

Test conditions to generate RS-343A standard video signals (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 147 ohms, VREF = 1.235v, SETUP = 7.5 IRE, 475/471* (477/471*) pin = logical one. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

Note: When using the internal voltage reference, RSET may need to be adjusted to meet these limits. Also, the "gray-scale" output current (white level relative to black) will have a typical tolerance of ± 10% rather than the ± 5% specified above.

*Since the Bt475 have 6-bit DACs (and the Bt477 in the 6-bit mode), the output levels are approximately 1.5% lower than these values.

A.C. Characteristics

		80 MHz Devices			66 MHz Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Clock Rate	Fmax			80			66	MHz
RS0 - RS2 Setup Time	1	10			10			ns
RS0 - RS2 Hold Time	2	10			10			ns
RD* Asserted to Data Bus Driven	3	5			5			ns
RD* Asserted to Data Valid	4			40			40	ns
RD* Negated to Data Bus 3-Stated	5			20			20	ns
Read Data Hold Time	6	5			5			ns
Write Data Setup Time	7	10			10			ns
Write Data Hold Time	8	10			10			ns
RD*, WR* Pulse Width Low	9	50			50			ns
RD*, WR* Pulse Width High	10	4*p13			4*p13			ns
Pixel and Control Setup Time	11	3			3			ns
Pixel and Control Hold Time	12	3			3			ns
Clock Cycle Time (p13)	13	12.5			15.15			ns
Clock Pulse Width High Time	14	4			5			ns
Clock Pulse Width Low Time	15	4			5			ns
Analog Output Delay	16			30			30	ns
Analog Output Rise/Fall Time	17		3			3		ns
Analog Output Settling Time*	18		13			13		ns
Clock and Data Feedthrough*			- 30			- 30		dB
Glitch Impulse*			75			75		pV - sec
DAC to DAC Crosstalk			- 23			- 23		dB
Analog Output Skew				2			2	ns
SENSE* Output Delay	19		1			1		µS
Pipeline Delay		4	4	4	4	4	4	Clocks
VAA Supply Current**	IAA							
normal operation								
sleep mode***			180	tbd		180	tbd	mA
clock enabled			10	tbd		10	tbd	mA
clock inhibited			1	tbd		1	tbd	mA

See test conditions on next page.

A.C. Characteristics (continued)

		50 MHz Devices			35 MHz Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Clock Rate	Fmax			50			35	MHz
RS0 - RS2 Setup Time	1	10			10			ns
RS0 - RS2 Hold Time	2	10			10			ns
RD* Asserted to Data Bus Driven	3	5			5			ns
RD* Asserted to Data Valid	4			40			40	ns
RD* Negated to Data Bus 3-Stated	5			20			20	ns
Read Data Hold Time	6	5			5			ns
Write Data Setup Time	7	10			10			ns
Write Data Hold Time	8	10			10			ns
RD*, WR* Pulse Width Low	9	50			50			ns
RD*, WR* Pulse Width High	10	4*p13			4*p13			ns
Pixel and Control Setup Time	11	3			3			ns
Pixel and Control Hold Time	12	3			3			ns
Clock Cycle Time (p13)	13	20			28			ns
Clock Pulse Width High Time	14	6			7			ns
Clock Pulse Width Low Time	15	6			9			ns
Analog Output Delay	16			30			30	ns
Analog Output Rise/Fall Time	17		3			3		ns
Analog Output Settling Time*	18		20			28		ns
Clock and Data Feedthrough*			- 30			- 30		dB
Glitch Impulse*			75			75		pV - sec
DAC to DAC Crosstalk			- 23			- 23		dB
Analog Output Skew				2			2	ns
SENSE* Output Delay	19		1			1		µS
Pipeline Delay		4	4	4	4	4	4	Clocks
Average VAA Supply Current**	IAA							
normal operation								
sleep mode***			180	tbd		180	tbd	mA
clock enabled			10	tbd		10	tbd	mA
clock inhibited			1	tbd		1	tbd	mA

See test conditions on next page.

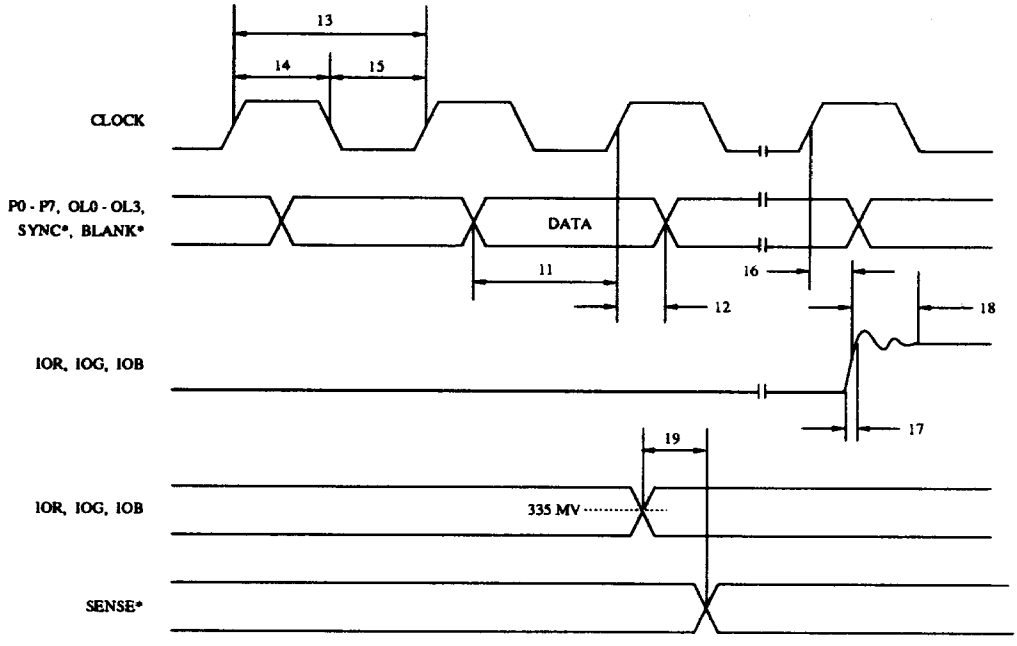
A.C. Characteristics (continued)

Test conditions (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 147 ohms, VREF = 1.235v, SETUP = 7.5 IRE, 475/471* (477/471*) pin = logical one. TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF. SENSE*, D0 - D7 output load ≤ 50 pF. See timing notes in Figure 7. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

*Clock and data feedthrough is a function of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the digital inputs have a 1k-ohm resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, -3 dB test bandwidth = 2x clock rate.

**At Fmax. IAA (typ) at VAA = 5.0v. IAA (max) at VAA (max).

***External current or voltage reference disabled during sleep mode.



Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.

Note 2: Settling time measured from the 50% point of full scale transition to the output remaining within ± 1 LSB (Bt477) or ± 1/4 LSB (Bt475).

Note 3: Output rise/fall time measured between the 10% and 90% points of full scale transition.

Figure 7. Video Input/Output Timing.

Timing Waveforms

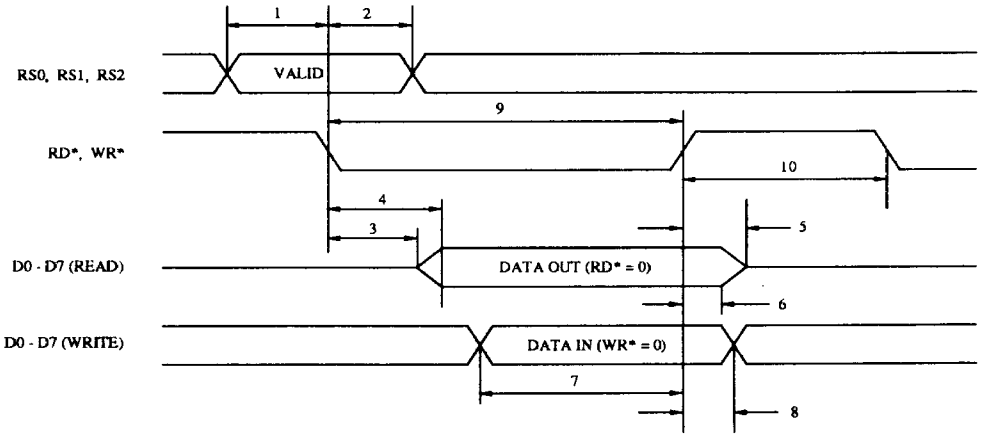


Figure 8. MPU Read/Write Timing.

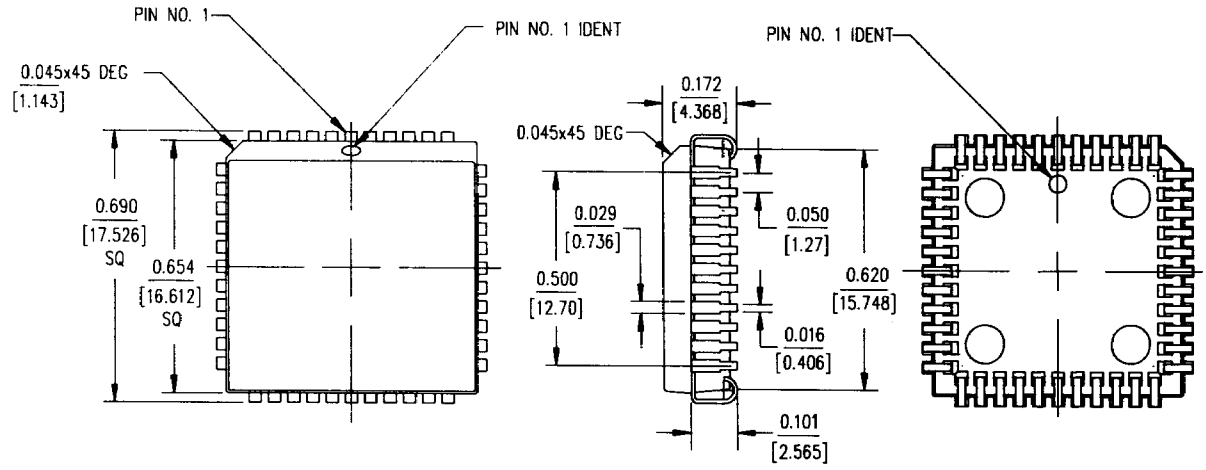
Ordering Information

Model Number	Color Palette RAM	Overlay Palette	Speed	Package	Ambient Temperature Range
Bt475KPJ80	256 x 18	15 x 18	80 MHz	44-pin Plastic J-Lead	0° to +70° C.
Bt475KPJ66	256 x 18	15 x 18	66 MHz	44-pin Plastic J-Lead	0° to +70° C.
Bt475KPJ50	256 x 18	15 x 18	50 MHz	44-pin Plastic J-Lead	0° to +70° C.
Bt475KPJ35	256 x 18	15 x 18	35 MHz	44-pin Plastic J-Lead	0° to +70° C.
Bt477KPJ80	256 x 24	15 x 24	80 MHz	44-pin Plastic J-Lead	0° to +70° C.
Bt477KPJ66	256 x 24	15 x 24	66 MHz	44-pin Plastic J-Lead	0° to +70° C.
Bt477KPJ50	256 x 24	15 x 24	50 MHz	44-pin Plastic J-Lead	0° to +70° C.
Bt477KPJ35	256 x 24	15 x 24	35 MHz	44-pin Plastic J-Lead	0° to +70° C.

Revision History

Revision	*Change from Previous Revision*
B	Bt475 added to specification.

Package Drawing -- 44-pin Plastic J-Lead (PLCC)



NOTES - Unless otherwise specified:

1. Dimensions are in inches [millimeters].
2. Tolerances are: .xxx ± 0.005 [0.127].
3. PLCC packages are intended for surface mounting on solder lands on 0.050 [1.27] centers.

CAUTION

ESD sensitive device. Permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.

Do not insert this device into powered sockets. Remove power before insertion or removal.

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