WARRANTY INFORMATION

Quatech Inc. warrants the **MPA-2000 /3000** to be free of defects for **one (1) year** from the date of purchase. Quatech Inc. will repair or replace any board that fails to perform under normal operating conditions and in accordance with the procedures outlined in this document during the warranty period. Any damage that results from improper installation, operation, or general misuse voids all warranty rights.

Although every attempt has been made to guarantee the accuracy of this manual, Quatech Inc. assumes no liability for damages resulting from errors in this document. Quatech Inc. reserves the right to edit or append to this document at any time without notice.

Please complete the following information and retain for your records. Have this information available when requesting warranty service.

DATE OF PURCHASE: _____

MODEL NUMBER: **MPA-2000/3000**

PRODUCT DESCRIPTION: **SINGLE CHANNEL EIA-530 SYNC. COMMUNICATIONS ADAPTER**

SERIAL NUMBER: _____

Table of Contents

Table of Figures

Section1 Introduction

The Quatech MPA-2000/3000 is a single channel, synchronous EIA-530 compatible serial communication port for systems utilizing the Micro Channel architecture. The MPA-2000 is RS-422 compatible and complies with the EIA-530 standard.

The MPA-300 has RS-485 data line drivers and receivers in place of the MPA-200's RS-422 drivers and receivers. While not fully compatible with the EIA-530 standard, the MPA-3000's RS-485 interface will allow multiple systems to connected in a multidrop configuration. Hereafter, the MPA2000/3000 will be referred to as the MPA-2000.

The port map of the MPA-2000 occupies a 16 byte block of I/O address space. The base address of this block may be located anywhere within the first 4 kilobytes (0 - 0FFFH) of available I/O address space in the system.

The MPA-2000 is available with a variety of serial communications controllers (SCC). All of the available SCC's can support asynchronous formats, byte-oriented protocols such as IBM Bisync, and bit-oriented protocols such as HDLC and IBM SDLC. The SCC's also offer internal functions such as on-chip baud rate generators, and digital phase-lock loops (DPLL). Refer to the appendices for further information on the SCC being used.

Addressing, direct memory access (DMA) channel, and interrupt level selections are made through the Programmable Option Select (POS) registers. These registers are programmed using the reference disk setup utilities that configure your Micro Channel system, and the Quatech installation utility, QTINSTAL.EXE (See Appendix 3-Additional Addressing, page 33) .

Section2 Board Description

The MPA-2000/3000 consists of and 8530 Serial Communications

circuitry that interfaces the SCC to the bus, and EIA-530 compatible driver circuitry.

data, generates interrupts and DMA requests, and also controls all activity on the communication line. The SCC is labeled U14 on the circuit board.

for most of the Micro Channel interfacing. Use of this integrated circuit allows for greater flexibility in control of the direct memory access (DMA)

circuit board.

External connections are made through a male D-25 connector CN2

CN1 if configured for data communications equipment (DCE). These configurations are installed at the time of manufacturing.

J2 and J3. The jumper block J3 selects the DMA request channel of the SCC, while jumper block J2 sets the source for enabling the driver circuitry.

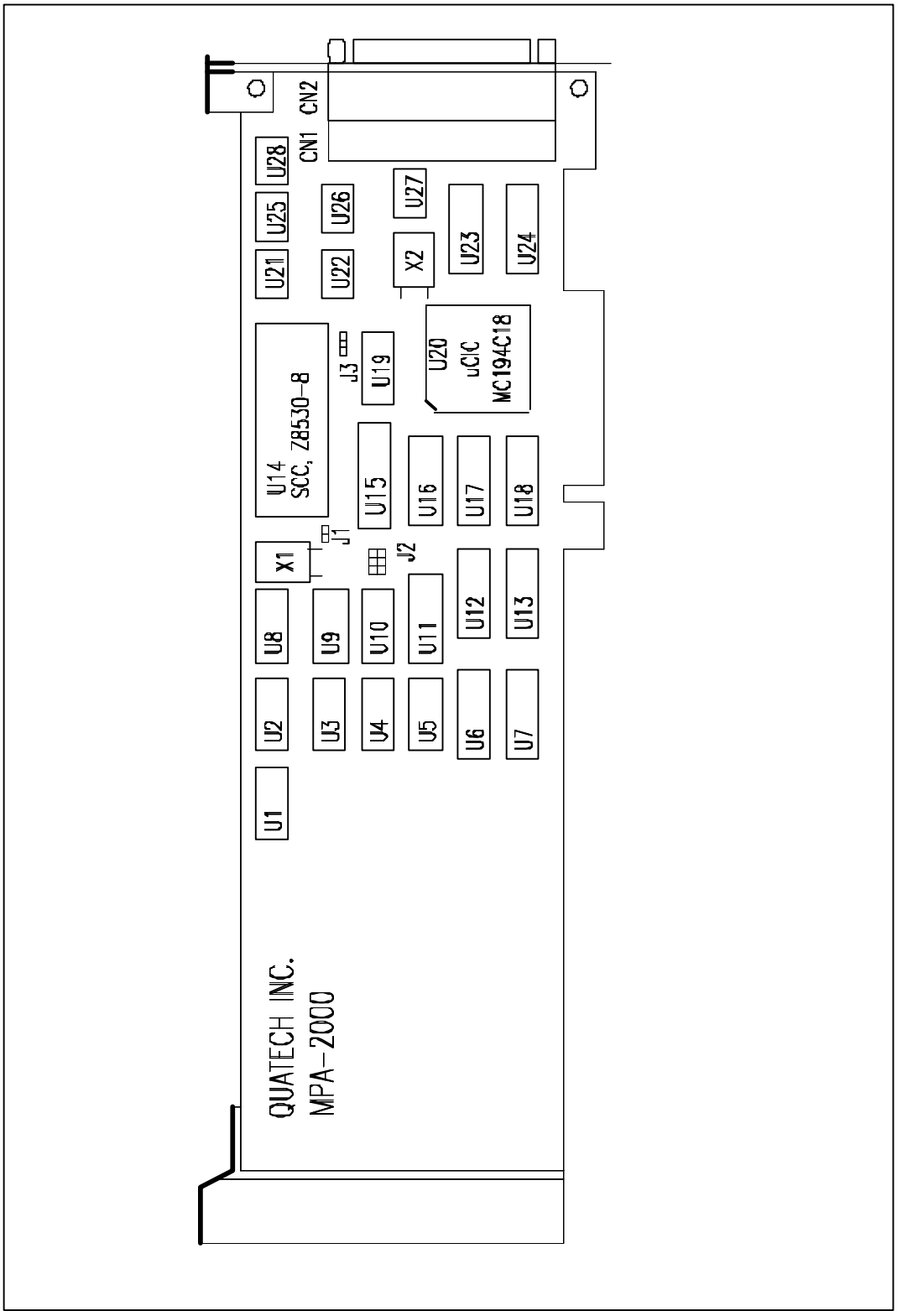
The driver circuitry for the MPA-2000 consists of three RS-423 drivers (U25, U27, U28), one RS-423 receiver (U26), four RS-422

(R5 - R6, R11 - R13). Resistor ROPT1 depends on the configuration and is installed at the time of manufacturing.

drivers (U25, U27, U28), one RS-485 receiver (U26), four RS-485 transceivers (U21, U22, U23, U24) and five 150 ohm termination resistors

and is installed at the time of manufacturing.

Figure1 MPA-2000 board drawing



Section3 SCC General Information

The Serial Communications Controller (SCC) is a dual channel, multi-protocol data communications peripheral. The SCC functions as a serial to parallel, parallel to serial converter/controller. The SCC can be software configured to satisfy a wide variety of serial communications applications. Some of its capabilities include:

1) Asynchronous
   - 5, 6, 7, or 8 bits per character
   - 1, 1-1/2, or 2 stop bits
   - Odd, even, or no parity
   - Times 1, 16, 32, or 64 clock modes
   - Break generation and detection
   - Parity, overrun and framing error detection

2) Byte-oriented Synchronous
   - Internal/external character synchronization
   - 1 or 2 sync characters in separate registers
   - Automatic Cyclic Redundancy Check (CRC) generation/detection

3) SDLC/HDLC
   - Abort sequence generation and checking
   - Automatic zero insertion and deletion
   - Automatic flag insertion between messages
   - Address field recognition
   - I-field residue handling
   - CRC generation and detection
   - SDLC loop mode with EOP recognition/loop entry and exit

4) NRZ, NRZI, or FM encoding/decoding

The mode of communication desired is established and monitored through the bit values of the internal read and write registers. The register set

only occupy four address locations, which start at Base + 0.

There are two register locations per SCC channel, a data port and a

requires loading a register pointer to perform the addressing to the correct data register. The first step is to write to the control port the operation and

read data from or write data to the control port. The only exception to this rule is when accessing the transmit and receive data buffers. These registers

single read or write to the data port. The following examples illustrate how to access the internal registers of the SCC. Also, Table 1 describes the read

The MPA-2000 accommodates CPU wait states during SCC accesses. Also, an on-board hardware timer will insert wait states on back

requirements of the SCC are met. This frees the application from needing to concern itself with these matters (This is usually accomplished by inserting

Example 1: Enabling the transmitter on channel A.

```
mov     dx,base     ; load base address
add     dx,1        ; add control reg a offset
mov     al,05h      ; write the register number
out     dx,al
mov     al,08H      ; write the register value
out     dx,al
```

Example 2: Monitoring the status of the transmit and receive buffers in RR0 of channel A. Note tht RR0 is directly accessed by default if no address is written to WR0.

```
mov     dx,base     ; load base address
add     dx,ContA    ; add control reg a offset
in      al,dx
```

Example 3: Write data into the transmit buffer of channel A.

```
mov     dx,base     ; load base address
out     dx,al       ; write data in ax to buffer
```

Example 4: Read data from the receive buffer of channel A.

```
mov     dx,base     ; load base address
in      al,dx       ; write data in ax to buffer
```

Table1 SCC read register description.

RR0	Transmit and receive buffer statuses, and external status

RR1	Special receive condition status, residue codes, error conditions
RR2	Modified channel B interrupt vector and unmodified channel A interrupt vector
RR3	Interrupt pending bits
RR8	Receive buffer
RR10	Miscellaneous status parameters
RR12	Lower byte of baud rate time constant
RR13	Upper byte of baud rate time constant
RR15	External/status interrupt information

The SCC can work with three forms of I/O operations: polling, interrupts, and block transfer. Polling transfers data, without interrupts, by

receiver, the transmitter, or External/Status conditions. Block transfer mode accommodates CPU wait states and DMA transfers. Further information on

The SCC incorporates additional circuitry to aid in serial communications. This circuitry includes clocking options, baud rate

programmed to select one of several sources to provide the transmit and receive clocks. These clocks can be programmed in WR11 to come from

MPA-2000 uses the TRXC pin for its clock-on-transmit and the RTXC pin for its clock-on-receive. Programming of the clocks should be done before

Table 2 SCC write register description.

WR0	Command register, register pointer, CRC initialization, resets for various modes
WR1	Interrupt control, RDY/DMA request control
WR2	Interrupt vector
WR3	Receiver initialization and control
WR4	Transmit/receive miscellaneous parameters and codes, clock rate, stop bits, parity
WR5	Transmitter initialization and control
WR6	Sync character (1st byte) or SDLC address field
WR7	Sync character (2nd byte) or SDLC Flag
WR8	Transmit buffer
WR9	Master interrupt control and reset
WR10	Miscellaneous transmitter/receiver control bits, NRZI, NRZ, FM coding, CRC reset
WR11	Clock mode and source control
WR12	Lower byte of baud rate time constant
WR13	Upper byte of baud rate time constant
WR14	Miscellaneous control bits: baud rate generator, DPLL control, auto echo
WR15	External/status interrupt control

For complete information regarding the SCC registers please refer to the manufacturer's data sheet for the specific part being used.

Baud Rate Generator Programming

The baud rate generator of the SCC consists of a 16-bit down counter, two 8-bit time constant registers, and an output divide-by-two. The time constant for the BRG is programmed in WR12 (least significant byte) and WR13 (most significant byte). The equation relating the baud rate to the time constant is given below while Table 3 shows the time constants associated with a number of common baud rates assuming a 6 MHz clock.

$$Baud\_Const = \frac{Clock\_Frequency}{2 * Buad\_Rate * Clock\_Mode} - 2$$

Clock_Frequency = crystal frequency of X1

Clock_Mode = value programmed in WR4

Baud_Rate = desired baud rate

Table3 Time constants for common baud rates

Baud Rate	Time Constant (Hex)
38,400	004CH
19,200	009AH
9,600	0136H
4,800	026FH
2,400	04E0H
1,200	09C2H
600	1386H
300	270EH

(for 6 MHz Clock)

SCC Data Encoding Methods

The SCC provides four different data encoding methods, selected by bits D6 and D5 in WR10. These four include NRZ, NRZI, FM1 and FM0. The SCC also features a digital phase-locked loop (DPLL) that can be programmed to operate in NRZI or FM modes. Also, the SCC contains two features for diagnostic purposes, controlled by bits in WR14. They are local loopback and auto echo.

For further information on these subjects or any others involving the SCC, refer to the appendix or contact the manufacturer of the SCC being used for a complete technical manual.

Section4 Jumper Block Configurations

The MPA-2000 utilizes two user configurable jumper blocks labeled J2 and J3, that allow the user more flexibility when configuring the board. The following section explains the function of each of the jumper blocks on the MPA-2000.

J2 - Driver Control Selection

J2 controls the source for enabling the driver circuitry on the MPA-2000. by selecting pins 1-2, the line drivers on the MPA-2000 will always be enabled. If the user wants the ability to enable and disable the drivers, pines 2-3 should be selected. By doing this, the drivers are controlled by bit D0 of the communications register. Similarly, by selecting pins 4-5 the receivers on the MPA-2000 will always be enabled. if pins 5-6 are selected, the receivers are controlled by bit D1 of the Communications register. Table 4 summarizes the jumper block selections for J2.

Table 4 Jumper block J2 Selections

Driver Function	Pins
Drivers and Receivers Always Enabled	1-2, 4-5
Drivers and Receivers controller by Communications Register, D0 and D1	2-3, 5-6

J3 - DMA REQ2 Source Selection

Jumper J3 controls the source for DMA REQ2. By setting J3 to 1-2 the source for REQ2 is the DTR/REQA pin of the SCC. This selection allows the transmit DMA requests for channel A to route through REQ2 for full duplex operation of channel A (Note, DTR/REQA may only be used with transmit DMA requests). Setting jumper J3 to 2-3 will route the RDY/REQB signals to DMA REQ2. The MPA-2000 only allows receiving of data on channel B. However, this allows for a fuller implementation of the EIA-530 standard under full duplex DMA operation by freeing up DTR/REQA for DTR functions. Full duplex DMA operation under this configuration forces the use of channel A for transmit and channel B for receive.

Table 5 Jumper J3 determining DMA REQ2 source

DMA Function	Pins
DTR/REQA for transmit	1-2
RDY/REQB for receive	2-3

Section5 Addressing

The MPA-2000 occupies a continuous 16 byte block of I/O addresses. For example, if the base address is set to 300H, then the MPA-2000 will occupy address locations 300H-30FH. The base address of the MPA-2000 may be set to any value in the first four kilobytes of I/O address space.

POS Register 103H Address Setup

in POS register 103H. This shown in Table 6, The base address of the MPA-2000 may be set to any of the first four kilobytes (0 - 0FFFH) of

into this register(The upper 4 bits of address are set to 0 by the hardare).

Note: this is a POS register and the address setup must be done using the your systems installation utilities and the Quatech address installation utility QTINSTAL.EXE. Setting this register using any other method could cause sytem confuration conflicts resulting in damage to your system.

Table6 POS 103H Bit Assignments, I/O Block Base Address

D7	D6	D5	D4	D3	D2	D1	D0
ADR11	ADR10	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4

The address range of the MPA-2000 is divided into two sections: communications and interfacing. The first 8 bytes of address space contain the internal registers of the SCC and the communications and configuration registers. The second 8 bytes of address space contain the internal registers of the µCIC. The entire address range of the MPA-2000 is shown in Table 7.

Table7 MPA-2000 Address Assignments

Address	Register Description
Base + 0	SCC Data Port, Channel A
Base + 1	SCC Control Port, Channel A
Base + 2	SCC Data Port, Channel B
Base + 3	SCC Control Port, Channel B
Base + 4	Communications Register
Base + 5	Reserved
Base + 6	Reserved
Base + 7	Reserved
Base + 8	µCIC internal I/O register 0
Base + 9	µCIC internal I/O register 1
Base + 10	µCIC internal I/O register 2
Base + 11	µCIC internal I/O register 3
Base + 12	µCIC internal I/O register 4
Base + 13	µCIC internal I/O register 5
Base + 14	Reserved
Base + 15	Reserved

Information on the internal registers of the SCC and the µCIC can be found in sections 3 and 10. The on-board communications register gives the user options pertaining to the EIA-530 standard. A detailed description of the communications register can be found in Section 8.

IRQ9. Selecting the interrupt level and the interrupt source is done through the µCIC internal POS register 104 using your reference disk setup utilities.

terminal count (INTTC), interrupt on test mode (INTTM), and interrupt from the SCC (INTSC). Interrupts from the SCC can occur on a number of conditions,

character received, interrupt on all characters received, interrupt on special condition received, interrupt on character transmitted, and interrupt on

The uCIC interface IC also comes into play during interrupt initialization and processing. First, the interrupts that are to be used must be

interrupt source on the MPA-2000 and also for the internal timer of the uCIC that must be set before interrupt servicing can begin. Seperate interrupt

by reading the uCIC interrupt status register, uCIC read register 3. Note that the status information is valid even when the uCIC interrupts are not

When interrupts are enabled and being serviced, they are latched by the uCIC (this is required of interrupts on the Micro Channel). Thus they must

3 of the uCIC. Note that this has no effect on the interrupt acknowledges that are also requred by the SCC. For additional information on these uCIC

and 25.

Note: It is important that all SCC interrupt sources are serviced before acknowledging the uCIC and exiting the Interrupt Service Routine. If an interrupt is still pending within the SCC and the uCIC is acknowledged and the ISR is exited, the MPA-2000 will no longer generate additional interrupts originating from the SCC.

When using interrupts with the MPA-2000, it is required that the

several things that an ISR must do to allow proper system operaion:

1. Do a software interrupt acknowledge to the SCC. This is accomplished by reading the interrupt vector register, status register 2, in channel B of the SCC. The value supplied by this read can also be used to vector to the appropriate part of the ISR.
2. Service the interrupt, IE, read the receiver buffer, write to the transmit buffer, etc.
3. Write a Reset Highest Interrupt Under Service (IUS) to the SCC. This is done by writing a 0x38 to the SCC command register.
4. Check for any additional interrutps pending in the SCC and service them.
5. Acknowledge the interrupt by writing to the uCIC interrupt acknowledge register.

For applications running under DOS, a non-specific End of Interrupt must be submitted to the interrupt controller. For Interrupts 2-7 this is done by writing a 0x20 to port 0x20. For Interrupts 10-12,14 and 15 this is done by writing a 0x20 to 0x60, then a 0x20 to 0x20 (Due to the interrupt controllers being cascaded). Note that this should only be done if it is a requirement of the operating system being used.

between an I/O devcice and memory, allowing for much faster data transfer rates. The MPA-2000 is equipped with two independent DMA request lines

To achieve DMA transfers with the MPA-2000 consideration must be given to the uCIC on the MPA-2000, and the SCC on the MPA-2000, and the

The UCIC contains several features facilitating DMA transfers. These include seperate enables for each reqeust, the abiliity to generate DMA

requests with hardware requests. On the MPA-2000 these requests come from the SCC. Also, the uCIC handles all DMA arbitration when the

For transmit DMA operations, the uCIC must be programmed with the hardware DMA request ANDed with the uCIC's software DMA request. With

uCIC receives a terminal count. Doing this will protect a system from inconsistencies that may arise at terminal count (TC). The Software DMA

DMA request being used.

For DMA request on transmit SCC should be programmed for DMA

DMA requests to come from either RDY/REQ or DTR/REQ. However, the MPA-2000 can only transmit from Channel A so that the SCC transmit DMA

RDY/REQA of channel A. DMA REQ2 utilizes DTR/REQA of channel A **only**

following the EIA-530 standard another source for DMA requests. Otherwise, this pin is used as the Data Terminal Ready (DTR) line and should not be

DMA transfers see the manufactorers data sheets.

After programming the uCIC and the SCC the system must be

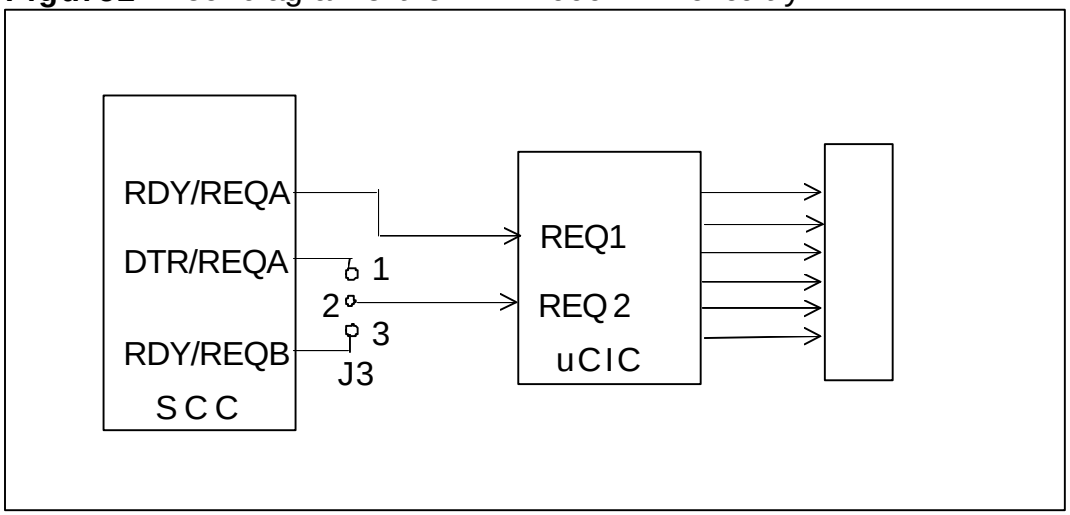
extended DMA modes must be used so the Port address of the data buffer can be programmed into the DMA controller. This is done last because it is

and uCIC only need programming during initialization. After the system DMA channel has been initialized, one should enabling the DMA on the SCC by

transmitted must be written manually, priming the SCC. This action satisfies certain internal timing requirements of the SCC. The DMA controller will then

transfer data from memory to the SCC on a request from the SCC. DMA requests are generated from the SCC when the transmit buffer of the SCC becomes empty.

Figure2 Block diagram of the MPA-2000 DMA circuitry



For DMA request on receive the SCC should be programmed for DMA request on receive for the desired request line. DMA REQ1 utilizes RDY/REQA of channel A. DMA REQ2 utilizes RDY/REQB of channel B **only** if pins 2-3 of jumper block J3 are selected. This gives the user another source for receive DMA requests. Note that to generate DMA requests off of channel B on receive, channel B must be used for data reception and fully programmed to do so.

After programming the SCC for DMA the system must be programmed for the DMA memory read transfers . For Miro Channel systems the extended DMA modes must be used so that the port address of the data buffer can be programmed into the DMA controller. After sytem initialization, enable the DMA on the SCC in WR1 and the the uCIC in write register 1. When a character enters the receive buffer of the SCC, a DMA request is generated. The DMA controller then writes the data from the SCC into memory.

Programming for full duplex operation with DMA on both transmit and receive is simply a combination of the two. There are two possible configurations that can be used, depending on the selection of jumper block J3. By selecting pins 1 & 2 of J3, REQ1 is used for DMA request on receive on RDY/REQA of channel A, and DMA REQ2 is used for DMA request on transmit on DTR/REQA of channel A. This configuration gives users not directly following the EIA-530 standard an optional way of performing DMA request on both transmit and receive. Otherwise, pins 2-3 of J3 should be selected. This configuration uses RDY/REQA of channel A as DMA REQ1 for DMA request on transmit, and uses RDY/REQB of channel B as DMA

REQ2 for DMA request on receive. Note that under this configuration, Channel B is used for receive.

The jumper block selections for J3 determining the source for DMA REQ2 are shown in Table 5, on page 9, while Figure 2 shows a block digram for the DMA circuitry of the MPA-2000.

Section8 Communications Register

The MPA-2000 is equipped with an on-board communications register which gives the user options pertaining to the clocks and testing. The user can specify the source and type of clock to be transmitted or received. Testing only pertains to a DTE and can be ignored if using a DCE. The following page contains a detailed description of the communications register and Table 8 details the bit information for this register.

Table8 Communication Register - Read/Write

D7	D6	D5	D4	D3	D2	D1	D0
0	0	LLEN	RLEN	RCKEN	TCKEN	RXDEN	TXDEN

D7-D6: Reserved, Always zero.

D5 Local Loop Back Enable (DTE only) (LLEN)

When set (logic 1), this bit allows the DTE to test the functioning of the DTE/DCE interface and the transmit and receive sections of the local DCE. When cleared (logic 0), no testing occurs.

D4 Remote Loop Back Enable (DTE only) (RLEN):

When set (logic 1), this bit allows the DTE to test the transmission path up to and through the remote DCE to the DTE interface and the similar return transmission path. When cleared (logic 0), no testing occurs.

D3 Receive Clock Enable (DCE only) (RCKEN):

When set (logic 1), this bit allows the DCE to transmit its clock-on-receive (RCLK). When cleared (logic 0), the DCE receives its RCLK. Since a DTE can only receive its RCLK, writing to this bit has no effect on a DTE.

D2 Transmit Clock Enable (DTE only) (TCKEN):

When set (logic 1), this bit allows the DTE to transmit its clock-on-transmit (TCLK). When cleared (logic 0), the DTE receives its TCLK. Since a DCE can only transmit its TCLK, writing to this bit has no effect on a DCE.

D 1 Receiver Enable (RXDEN):

When set (logic 1), along with selecting pins 2-3 of J2, this bit enables the receivers on the MPA-2000.

D 0 Transmitter Enable (TXDEN):

When set (logic 1), along with selecting pins 5-6 of J2, this bit enables the drivers on the MPA-2000.

Section9 DTE/DCE Configuration Differences

(DTE) or Data Circuit-terminating Equipment (DCE). Both configurations possess some important similarities and differences on the MPA-2000 that

Both the DTE and the DCE configurations possess the user option of enabling and disabling the driver circuitry on the MPA-2000. This is

control over the driver circuity on the MPA-2000. See Section 4 Jumper Block Configurations for further information on the configuration of this

Another option that the DTE and DCE versions possess is the ability to receive data and clock-on-receive on channel B of the SCC. This gives the

The differences on the MPA-2000 between the DTE and the DCE configuration include signal definitions, control signals, clocking options and

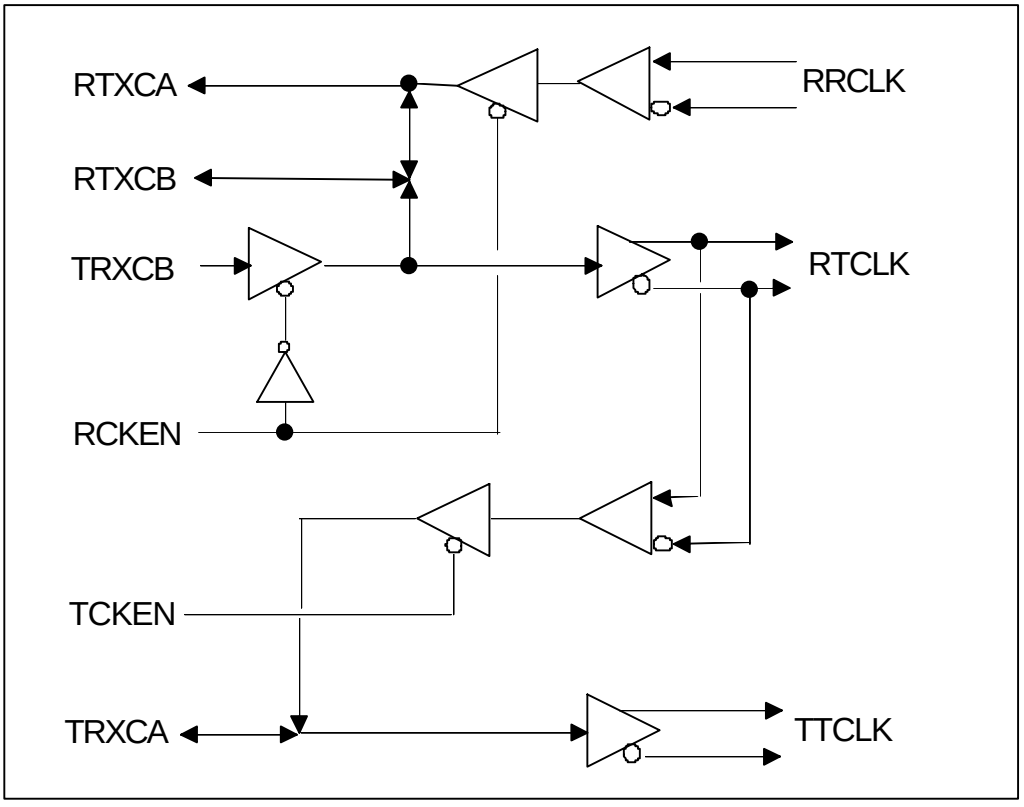
summarizes these differences.

DTE Configuration

The control signals the DTE can generate are the Ready to Send (RTS) and DTE Ready (DTR). It can receive the signals Carrier Detect (CD), Clear to Send (CTS), and DCE Ready (DCR). All the control signals are controlled through channel A of the SCC, with the exception of the DCR signal, which is received on DCDB on channel B.

The DTE can transmit its clock-on-transmit (TTCLK) from TRXCA pin (pin 14) on channel A of the SCC, receive its TCLK on the same pin (depending on bit D2 of the communications register) through the RTCLK pins, or receive its clock-on-receive (RRCLK) on RTXC pins (pins 12 & 28) on channels A and B of the SCC. The DTE can not transmit its RCLK. Figure 3 illustrates the clock circuitry of the MPA-2000 for it's DTE configuration.

Figure3 DTE clock configuration



The testing signals the DTE can generate are the Local Loop back Test (LL) and the Remote Loop Back Test (RL). These signals are generated from the on-board communications register. When a Test Mode (TM) condition is received, an interrupt can be generated on the DTE. Table 9 summarizes the signals on the DTE.

NOTE:
The Local Loopback Test and the Remote Loopback Test cannot be performed simultaneously. Thus, bits D5 and D4 of the communications register should not be set (logic 1) simultaneously.

Table9 DTE Signals

Signal	Received	Generated	Monitored
RTS		X	RTSA pin of SCC
CTS	X		CTSA pin of SCC
DTR		X	DTR/REQ of SCC
DCR	X		DCDB pin of SCC
CD	X		DCDA pin of SCC
TxCLK	X	X	TRXCA pin of SCC
RxCLK	X		RTXC pin of SCC
LL		X	Bit D5 of Comm. Reg
RL		X	Bit D4 of Comm Reg
TM	X		INTM or Bit D7 of Comm Reg

DCE Configuration

These signals still have the same representation for the DCE. The difference on the MPA-2000 is that the names given to each of the signals on the DCE

example, pin 2 of the DCE connector is received data, yet the signal is on the transmitted data line.

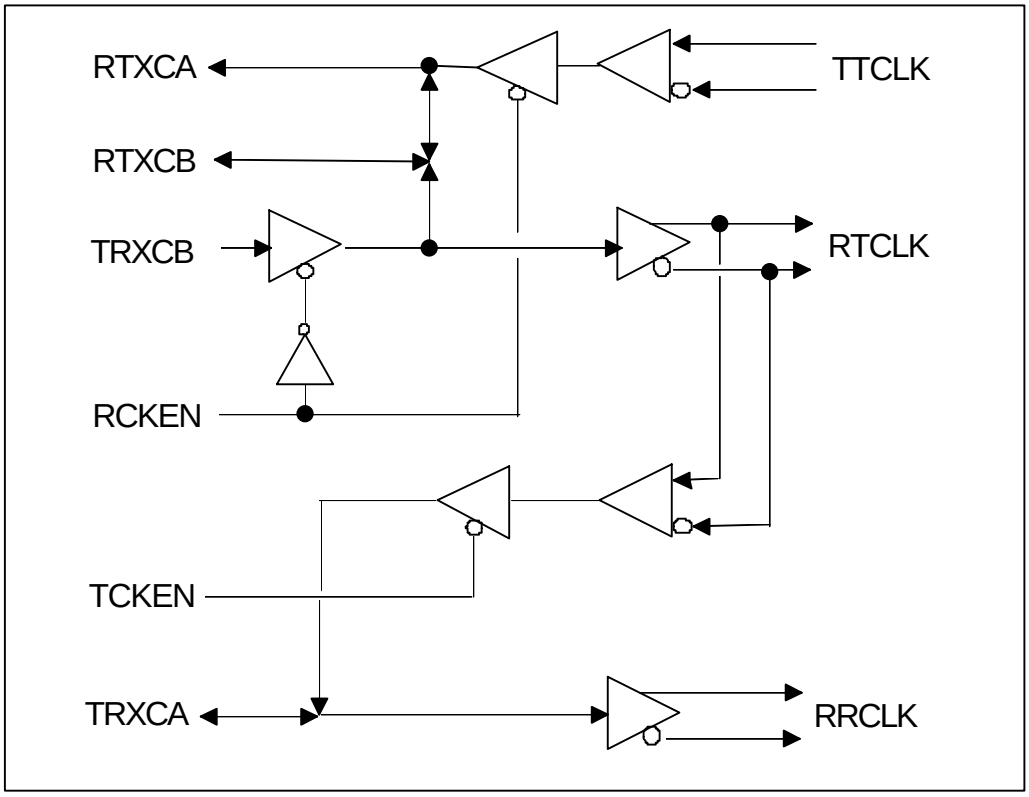
(CTS), Carrier Detect (CD), and DCE Ready (DCR). It can receive the signals DTE Ready (DTR) and Ready to Send (RTS). All the control signals

exception of the CD signal, which is generated from DTR/REQB on channel B.

channel A of the SCC, transmit its clock-on-receive (TRCLK) from TRXCB on channel B of the SCC (depending on bit D3 of the communications

register), or receive its clock-on-receive (RRCLK) on RTXC on channels A and B of the SCC. The DCE can not receive a TCLK. Figure 4 illustrates the clock circuitry of the MPA-2000 for it's DCE configuration.

Figure4 DCE clock configuration



The only testing signal the DCE can generate is the Test Mode (TM) signal, which is always in the OFF condition and cannot be changed by the user. The Local Loop back (LL) and Remote Loop Back (RL) test signals are not implemented on the DCE. Table 10 summarizes the signals on the DCE.

Table10 DCE Signals

Signal	Received	Generated	Monitored
RTS	X		CTSA pin of SCC
CTS		X	RTSA pin of SCC
DTR	X		DCDA of SCC
DCR		X	DTR/REQA pin of SCC
CD		X	DTR/REQB pin of SCC
TxCLK		X	TRXCA pin of SCC
RxCLK	X	X	RTXC/TRXCB pin of SCC
LL	-	-	Unused
RL	-	-	Unused
TM		X	D7 of Comm Reg

Section10 Programmable Option Select

Adapters designed for the Micro Channel Architecture utilize on board registers referred to as the Programmable Option Select (POS) registers to hold the adapter's configuration information. The first two POS registers hold a unique adapter identification number that has been issued to Quatech for the MPA-2000. This identification number is defined in the hardware and cannot be changed. These registers are read only. POS register 103 is also implemented on the board, but its contents are stored in the µCIC for read back purposes.

The three remaining POS registers on the MPA-2000 are internally implemented on the µCIC and are used for DMA and interrupt selections. These registers are programmed using the reference diskette supplied with your Micro Channel system and the Quatech address installation software QTINSTAL.EXE. Information on the uCIC POS registers can be found in Section 11, MCI94C18 Functional Description.

Section 11 MCI94C18 Functional Description

The Standard Microsystem's MCI94C18 Micro Channel Interface Circuit (µCIC) is a CMOS device that integrates many common functions of the Micro Channel Bus into a single 68 pin package. This significantly reduces the number of components required on the adapter board. In addition, the µCIC supports several high level functions of the Micro Channel bus.

The µCIC provides complete support for all eight POS registers according to the Micro Channel specification. Some of these registers are implemented on the chip while others are handled externally. POS registers 102, 104 and 105 are inside the µCIC and control the behavior of the chip. POS registers 100 and 101 (adapter ID), along with register 103 are placed on the adapter board. The contents of POS register 103 is stored in the µCIC for read back purposes. POS registers 106 and 107 are not implemented on the MPA-2000. Below is a description of the internal POS registers.

Table11 POS Port 102H Bit Definitions

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	DARB3	DARB2	DARB1	DARB0	CDEN

D7-D5 Reserved, always 0.

D4-D1 DMA Channel 1 Arbitration Level (4 bits - DARB#):

This field defines the DMA arbitration level to be associated with the DMA request line REQ1.

D0 Card Enable (CDEN):

This bit has to be set (logic 1) after all other POS registers are configured. It is the main hardware enable for the MCA interface for a particular adapter. All adapter I/O functions except for setup read and write accesses are disabled until this bit is set.

Table12 POS Port 104H Bit Definitions

D7	D6	D5	D4	D3	D2	D1	D0
INTTI Map		INTTM Map		INTSC Map		INTTC Map	

D7-D0 Interrupt Mapping:

The mapping bits specify the IRQn pin to be associated with each INTn interrupt input. Interrupts can be merged into a pin by assigning them the same mapping.

INTn MAP	MAPPED TO IRQn
00	IRQ3
01	IRQ9
10	IRQ5
11	IRQ7

Table13 POS Port 105H Bit Definitions

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	DARB3	DARB2	DARB1	DARB0

D7-D4 Always 0

D3-D0 DMA Channel 2 Arbitration Level (4 bits):

This field defines the DMA arbitration level to be associated with the DMA request line REQ2.

General Purpose I/O Registers

In addition to the internal POS registers, the µCIC includes six general purpose input/output registers. These registers control the operational

The internal registers of the µCIC start at an address location of Base + 8. This set of registers control the number of wait states generated for I/O

channels and their mode of operation, and the enabling, status and acknowledgement of the interrupt inputs. Below is a description of each of

I/O REGISTERS

Table14 uCIC Register 0 at Base + 8 (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
0	EnTimer	IOWT2	IOWT	IOWT0	0	0	0

D7 Always 0.

D6 Enable Timer (Entimer)

When set (logic 1), the programmable timer of the µCIC is enabled. The timer on the µCIC can be used to generate internal interrupts for time-out purposes.

D5-D3 Number Of I/O Wait States (3 bits - IOWT#):

These bits control the number of I/O wait states according to the table below. The MP-2000 will operate properly with this register set at the default value of 7 clocks. However, improved performance may be seen when operating high speed DMA transfers by setting to lower vaues.

Value	Behavior
7	No wait state - basic cycle
6	1 wait state - synchronous extended cycle
5 - 0	(7- Value) wait states Asynchronous extended cycle

D2-D0 Reserved, always 0

Table15 uCIC Register 1 at Base + 9 (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	EDMA2	EDMA1

D7-D2 Reserved, always 0

D1 Enable Dma Request 2 (EDMA2):

This bit enables DMA channel 2. On the MPA-2000 REQ2 is generated from DTR/REQA for transmit if jumper J3 is set to 1-2. REQ2 is generated from RDY/REQB for receive if jumper J3 is set to 2-3.

D0 Enable DMA Request 1 (EDMA1):

This bit enables DMA channel 1. On the MPA-2000 REQ1 is generated from RDY/REQA for transmit or receive depending on the DMA mode of the SCC.

Table16 uCIC Register 2 at Base + 10 (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
0	INTTI	0	INTTM	INTSC	INTTC	0	0

D7 Reserved, always 0

D6 Timer Interrupt Enable (InTT1):

When set (logic 1), this bit enables the timer interrupt. An interrupt will be generated when the timer up counter reaches 255.

D5 Reserved, always 0.

D4-D2 Interrupt Enable Bits (3 bits - INTTM, INTSC, INTTC):

These bits are used to individually enable or disable each of the three external interrupt sources. The sources include interrupt on terminal count (INTTC), interrupt from the SCC (INTSC), and interrupt on Test Mode (INTTM). When cleared (logic 0), the corresponding interrupt is disabled. If an interrupt does occur, it is prevented from causing an IRQ on the Micro Channel. However, that interrupt will still be stored, and its value can be polled using the interrupt status register. When set (logic 1), the µCIC allows the stored interrupt, or any following interrupt, onto the IRQ line determined by the mapping bits in POS register 104.

D1-D0 Reserved, always 0.

Table 17 uCIC Register 3 at Base + 11(Read)

D7	D6	D5	D4	D3	D2	D1	D0
ANY	INTTI	0	INTTM	INTSC	INTTC	0	0

D7 Any Interrupt (ANY):

This bit represents the OR function between the four interrupt sources.

D6 Timer Interrupt Status Bit (INTT1):

This bit reflects the state of the stored timer interrupt.

D5 Reserved, always 0

D4-D2 Interrupt Status Bits (3 Bits - INTTM, INTSC INTTC):

These bits reflect the state of each stored interrupt. It can be used for polling purposes, or to identify the source when the interrupts are merged.

D1-D0 Reserved, always 0

Table 18 uCIC Register 3 at Base + 11 (Write)

D7	D6	D5	D4	D3	D2	D1	D0
TMTST	INTT1	0	TMA	SCACK	TCACK	0	0

D7 Timer Test (TMTST):

This bit, when 1, scales down the timer to be a 4 bit counter.

D6 Timer Interrupt Acknowledge Bit (INTT1)

D5 Reserved, always 0

D4-D2 Interrupt Acknowledge Bits (3 Bits - TMA, SCACK,TCACK):

These bits are used to acknowledge each of the stored interrupt sources. Writing a one to any of the acknowledge bits clears the corresponding stored interrupt. Following interrupts will be normally stored.

D1-D0 Reserved, always 0

Table19 uCIC Register 4 at Base + 12 (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0

D7-D0 Timer Count Bits (8 bits - TC#):

These bits either write the starting value of the up counter or read the present count. The equation relating the frequency of the timer (FREQ) to the count (COUNT) is shown below.

$$FREQ = \frac{50MHz}{128 * (256 - COUNT)}$$

Note: This timer is not required by the MPA-2000 forf communications allowing it for use by the application.

Table20 uCIC Register 5 at Base + 13 (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
A/0 2	A/O 1	0	0	0	0	S/W 2	S/W 1

D7-D6 AND/OR DMA Requests 2,1 (2 bits- A/O#):

Each bit specifies whether the software and the hardware DMA requests of the corresponding channel are ANDed or ORed. However, the MPA-2000 only utilizes the ANDing of the two requests. When set (logic 1), the requests (REQ) are ANDed which protects the system from inconsistencies that may arise at terminal count (TC). Regardless of whether the SCC removes its REQ signal at the end of a DMA transfer session, the Software DMA Request bit is reset on TC guaranteeing that the hardware REQ is ignored. Thus, the bit corresponding to the desired REQ line should always be set (logic 1) when using DMA.

D5-D2 Reserved, always 0

D1-D0 Software DMA Request 2,1 (2 bits - S/W#):

When set (logic 1), these bits initiate a software DMA request on the corresponding channel. Each bit will be automatically cleared by a terminal count while its channel has the bus. A software DMA request can be withdrawn by writing a logic 0 into these bits.

Section12 External Connections

The MPA-2000 is designed to meet the EIA-530 standard through a D-25 connector. When configured as a DTE, the MPA-2000 uses a D-25 short body male connector (labeled CN2). When configured as a DCE, the MPA-2000 uses a D-25 long body female connector (labeled CN1). Table 21 defines the pin definitions for both connectors and Figures 5 and 6 illustrate the pin-outs for each of the connectors. The definitions of the interchange circuits according to the EIA-530 standard follows.

Table21 Connector Pin Definitions

Pin	DTE	Circuit	DCE	Circuit
1	CGND	-	-	-
2	+TXD	BA	+RXD	BB
3	+RXD	BB	+TXD	BA
4	+RTS	CA	+CTS	CB
5	+CTS	CB	+RTS	CA
6	+DCR	CC	+DTR	CD
7	DGND	AB	DGND	AB
8	+CD	CF	+CD	CF
9	-RRCLK	DD	-TTCLK	DA
10	-CD	CF	-CD	CF
11	-TTCLK	DA	-RRCLK	DD
12	-RTCLK	DB	-RTCLK	DB
13	-CGS	CB	-RTS	CA
14	-TXD	BA	-RXD	BB
15	+RTCLK	DB	+RTCLK	DB
16	-RXD	BB	-TXD	BA
17	+RRCLK	DD	+TTCLK	DA
18	LLBK	LL	-	-
19	-RTS	CA	-CTS	CB
20	+DTR	CD	+DCR	CC
21	RLBK	RL	-	-
22	-DCR	CC	-DTR	CD
23	-DTR	CD	-DCR	CCC
24	+TTCLK	DA	+RRCLK	DD
25	TEST MODE	TM	TESTMODE	TM

Figure5 MPA-2000 DTE Output Connector

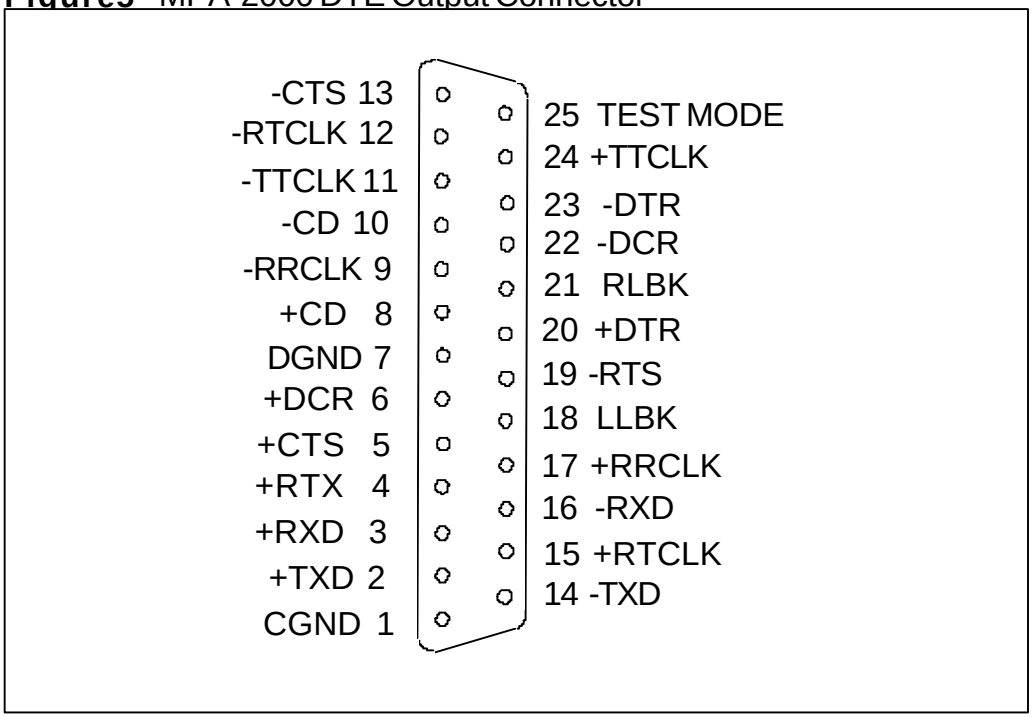
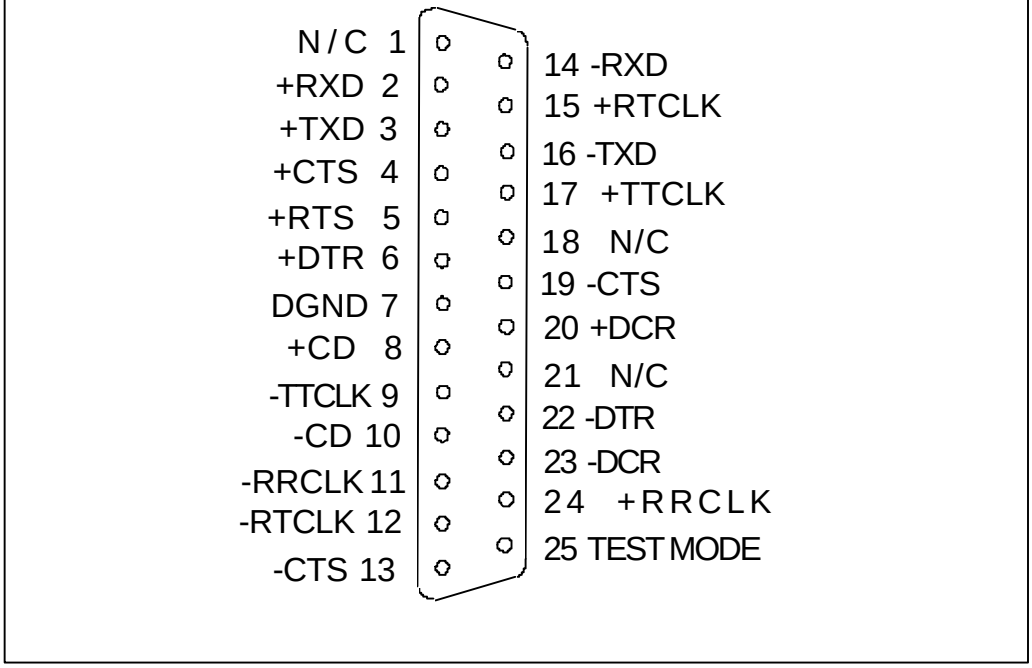


Figure6 MPA-2000 DCE Output Connector



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Appendix1 DEFINITIONS OF INTERCHANGE CIRCUITS

CIRCUIT AB - SIGNAL GROUND

- CONNECTOR NOTATION: DGND
- DIRECTION: Not applicable

This conductor directly connects the DTE circuit ground to the DCE circuit ground.

CIRCUIT CC - DCE READY (Data Set Ready)

- CONNECTOR NOTATION: +DCR,-DCR
- DIRECTION: From DCE

This signal indicates the status of the local DCE by reporting to the DTE device that a communication channel has been established.

CIRCUIT BA - TRANSMITTED DATA

- CONNECTOR NOTATION: +TXD,-TXD
- DIRECTION: To DCE

This signal transfers the data generated by the DTE through the communication channel to one or more remote DCE data stations.

CIRCUIT BB - RECEIVED DATA

- CONNECTOR NOTATION: +RXD,-RXD
- DIRECTION: From DCE

This signal transfers the data generated by the DCE, in response to data channel line signals received from a remote DTE data station, to the DTE.

CIRCUIT DA - TRANSMIT ELEMENT TIMING **(DTE Source)**

- CONNECTOR NOTATION: +TTCLK,-TTCLK
- DIRECTION: To DCE

This signal, generated by the DTE, provides the DCE with element timing information pertaining to the data transmitted by the DTE. The DCE can use this information for its received data.

CIRCUIT DB - TRANSMIT ELEMENT TIMING (DCE Source)

- CONNECTOR NOTATION: +RTCLK,-RTCLK
- DIRECTION: From DCE

This signal, generated by the DCE, provides the DTE with element timing information pertaining to the data transmitted by the DTE.

CIRCUIT DD - RECEIVER ELEMENT TIMING (DCE Source)

- CONNECTOR NOTATION: +RRCLK,-RRCLK
- DIRECTION: From DCE

This signal, generated by the DCE, provides the DTE with element timing information pertaining to the data transmitted by the DCE. The DTE can use this information for its received data.

CIRCUIT CA - REQUEST TO SEND

- CONNECTOR NOTATION: +RTS,-RTS
- DIRECTION: To DCE

This signal controls the data channel transmit function of the local DCE and, on a half-duplex channel, the direction of the data transmission of the local DCE.

CIRCUIT CB - CLEAR TO SEND

- CONNECTOR NOTATION: +CTS, -CTS
- DIRECTION: From DCE

This signal indicates to the DTE whether the DCE is conditioned to transmit data on the communication channel.

CIRCUIT CF - CARRIER DETECT

- CONNECTOR NOTATION: +CD, -CD
- DIRECTION: From DCE

This signal indicates to the DTE whether the DCE is conditioned to receive data from the communication channel, but does not indicate the relative quality of the data signals being received.

CIRCUIT CD - DTE READY (Data Terminal Ready)

- CONNECTOR NOTATION: +DTR, -DTR
- DIRECTION: To DCE

This signal controls the switching of the DCE to the communication channel. The DTE will generate this signal to prepare the DCE to be connected to or removed from the communication channel.

CIRCUIT LL - LOCAL LOOP BACK

- CONNECTOR NOTATION: LLBK
- DIRECTION: To DCE

This signal provides a means whereby a DTE may check the functioning of the DTE/DCE interface and the transmit and receive sections of the local DCE.

CIRCUIT RL - REMOTE LOOP BACK

- **CONNECTOR NOTATION: RLBK**
- DIRECTION: To DCE

This signal provides a means whereby a DTE or a facility test center may check the transmission path up to and through the remote DCE to the DTE interface and the similar return transmission path.

CIRCUIT TM - TEST MODE

- CONNECTOR NOTATION: TEST MODE
- DIRECTION: From DCE

This signal indicates to the DTE that the DCE is in a test condition. The DCE generates this signal when it has received a local loop back or remote loop back signal from the DTE.

According to the EIA-530 standard, the local loopback and remote loopback signals are optional and are omitted from the DCE configuration of the MPA-2000. Since testing will never occur for this configuration, the test mode signal will always be in the OFF condition for the DCE. These three test signals follow the EIA-423-A

Appendix2 HARDWARE INSTALLATION

Make sure there is a back-up copy of the original IBM PS/2 reference diskette available. A copy of the reference disk must be used for the installation process as the diskette must be modified to accept any option adapters. The following are steps for installing the MPA-2000.

1. Turn system unit off.
2. Remove system cover as instructed in the IBM Quick Reference Guide.
3. Insert adapter into any vacant slot following the guidelines for installing an option adapter in the IBM Quick Reference Guide.
4. Replace system cover.
5. Turn unit on and insert a COPY of the IBM PS/2 reference diskette into drive A.
6. Respond "N" at automatic configuration prompt.
7. Select "Copy an option diskette" and follow the copying instructions.
8. Select "Set configuration"
9. Select "Change configuration" or "Run automatic configuration" and follow the installation instructions.

NOTE:

When installing the MPA-2000, if the desired address is not available in the configuration routine, select any non-conflicting address and continue with Additional Addressing (section XII).

After the initial installation, the copy of the reference diskette will contain the configuration file for the MPA-2000. Subsequent re-installation may omit step 7 and a "Y" response may be given during step 6 (automatically configure system) if desired.

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Appendix3 Additional Addressing

The MPA-2000 supports the entire I/O address range of the PS/2 occupying 16 consecutive I/O locations. This produces 256 possible choices for a base address location. Since it would not be feasible or practical to provide all of these choices in the configuration file, 25 addresses have been selected for inclusion in the file. To simplify the configuration process, an address installation utility (QTINSTAL.EXE) has been included on the distribution diskette to facilitate the address installation process. QTINSTAL should be used

1. Insert the MPA-2000 distribution disk in drive A of the system.
2. Execute QTINSTAL.EXE
3. Select the MPA-2000 by using the cursor keys to highlight the selection and press <enter>. See figure 15.
4. At the prompt, insert the back-up copy of your systems reference disk in drive A.
5. Select an address to change by using the cursor keys to highlight the address and press <enter>. (Addresses will appear in ascending order.) See figure 16.
6. Enter the desired address in hex, decimal, or binary (hex is the default radix). See figure 17.
7. Repeat steps 5 and 6 as necessary.
8. Press <esc> to exit the address menu.
9. Press <enter> to save configuration changes. (A back-up copy of the configuration file will be generated). Or, press <esc> to exit without saving changes.
10. Press <esc> to exit the board selection menu.
11. Press <esc> to return to DOS. The configuration file is modified but the system configuration is not updated. Or, press <enter> to enter the IBM installation utilities and update the system configuration.

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Appendix4 Specifications

Controller:	Serial Communications Controller (determined by user, typically an Intel 82530)	
Interface:	DTE: short body male D-25 connector DCE: long body female D-25 connector	
Transmit drivers:	EIA-422: EIA-423:	75174 or compatible MC3488 or compatible
Receive buffers:	EIA-422: EIA-423:	75175 or compatible 75176 or compatible
Transceivers:	EIA-422:	75176 or compatible
I/O Address range:	0000H - 0FFFH	
Interrupt levels:	IRQ 3,5,7,9	

Power requirements:

I_{Typ} (mA)	I_{Max} (mA)	Supply Voltage (Volts)
1070	1202	5
25	36	12
25	36	-12