Advance Data Sheet

AT&T Microelectronics

T7220A Twisted-Pair Medium Attachment Unit (TPMAU2) Issue 0.2

Features

- Compliance with IEEE 802.3 standards* for AUI-interface
- Compliance with IEEE 802.3 10BASE-T standard
- Direct interface to AUI transformer and TP filters
- Internal predistortion generation
- Internal squelch circuits
- Selectable end-of-packet SQE_test
- Selectable link-integrity test with external LED indication
- LED control for transmit, receive, jabber, and collision
- Single 5 V supply and low-power CMOS technology
- Lower TP threshold option for extended range of applications
- Selectable autopolarity detection and correction function with LED indication

Description

The T7220A Twisted-Pair Medium Attachment Unit (TPMAU2) simplifies the design and implementation of a minimal-part-count, cost-effective medium attachment unit (MAU) between an Ethernet attachment unit interface (AUI) and the twisted-pair wire media. Ethernet users can now use twisted-pair wiring for LAN construction and/or expansion, and still use existing Ethernet-interface cards. A MAU built with the TPMAU2 provides the electrical interface between the Ethernet transceiver cable (IEEE AUI) and the twisted-pair wire.

Standard features of the TPMAU2 include level-shifted data passthrough from one transmission media to another, collision detection, and precise internal predistortion control signals. Additional features include selectable signal quality error (SQE) test generation, a squelch function, LED controls for IC status, link-integrity strapping option, and autopolarity detection and correction. A block diagram of the T7220A is shown in Figure 1. The T7220A TPMAU2 is fabricated by using linear CMOS technology and is available in a 28-pin, plastic DIP or SOJ package.

* IEEE 802.3i-1990.

August 1991

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Description (continued)

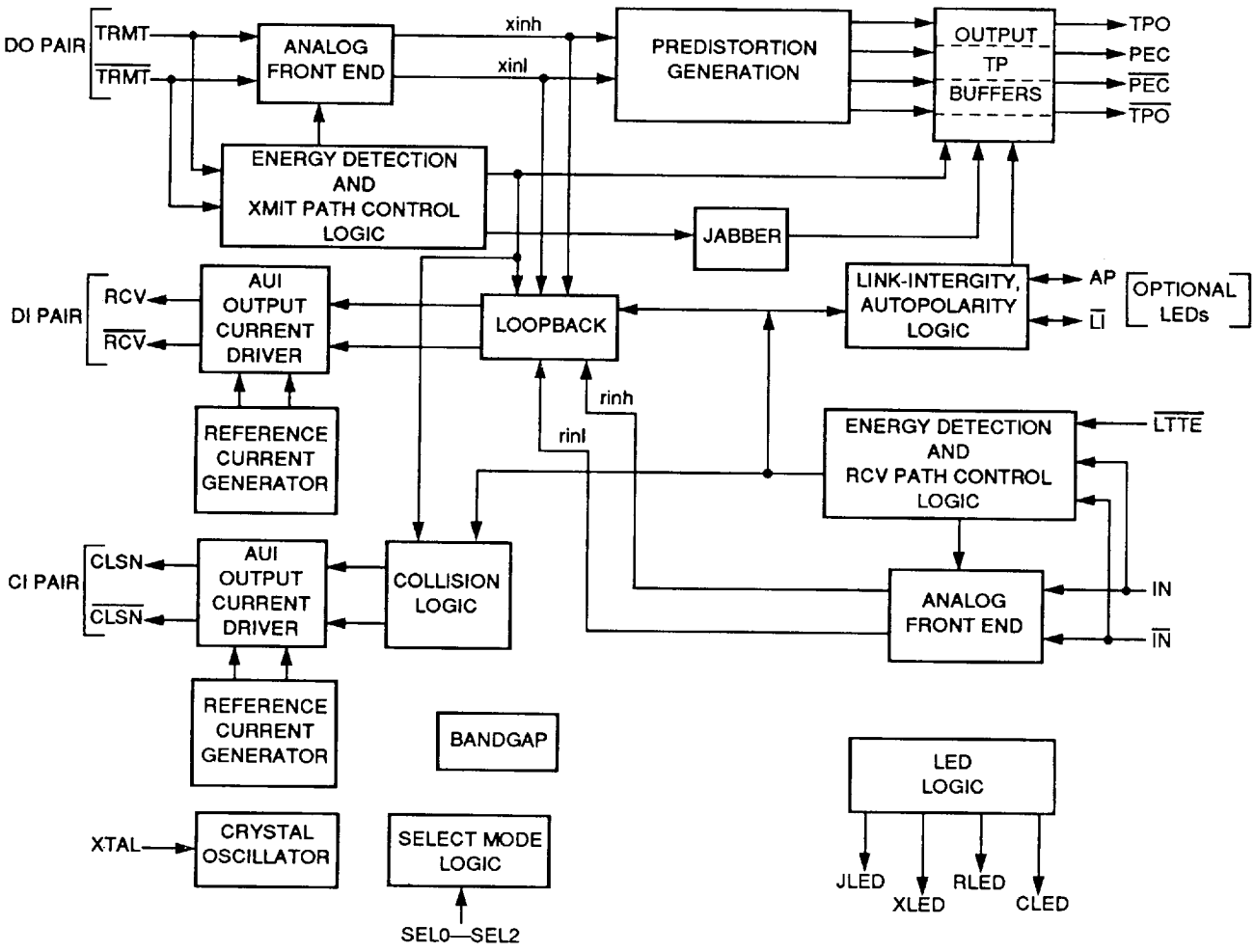


Figure 1. Block Diagram

Pin Information

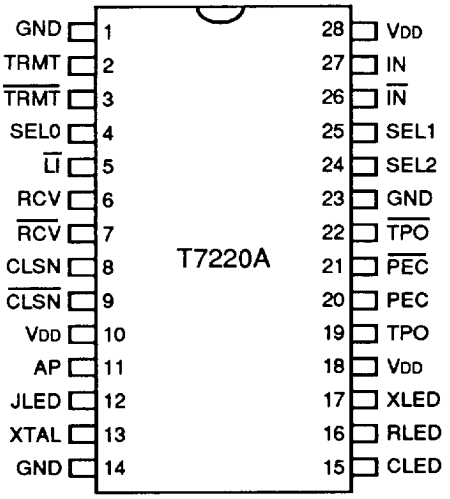


Figure 2. Pin Diagram

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Function
1, 14, 23	GND	—	**Ground.** All pins must be tied to the same ground potential point.
2, 3	TRMT, $\overline{\text{TRMT}}$	I	**Transmit Data Pair.** A differential receiver input pair from the DO circuit that receives 10 Mbits/s Manchester-encoded data from the AUI-transceiver cable, which is driven by the DTE (terminal or computer). The receiver should be isolated from the AUI-transceiver cable by a pulse transformer, as required by 802.3.*
4, 25, 24	SEL0 SEL1 SEL2	I I I	**Mode Select Pins.** These input pins select one of eight different modes of operation, as described in the Modes of Operation section. The reconfiguration is intended to remain backward compatible with the earlier T7220.
5	$\overline{\text{LI}}$	I/O	**Link-Integrity Enable.** This pin is a dual-function pin that determines if the link-integrity function should be realized. If properly configured, it provides a method to drive an LED and indicate the status of the link. The pin is also 100% backward compatible with the earlier version of the T7220.
6, 7	RCV, $\overline{\text{RCV}}$	O	**Receive Data Pair.** An output current driver pair to the DI circuit that drives the AUI-transceiver cable with the 10 Mbits/s Manchester-encoded data received from the twisted-pair wire of the network. This driver should be isolated from the AUI-transceiver cable by a pulse transformer, as required by 802.3.*

* Please consult *Using the T7220 Twisted-Pair Medium Attachment Unit (TPMAU) without the AUI Transformer* (TN90-013SMOS) for use of this device without an AUI isolation transformer.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin	Symbol	Type	Name/Function
8, 9	CLSN, $\overline{\text{CLSN}}$	O	**Collision Presence Pair.** An output current driver pair to the CI circuit that drives the AUI-transceiver cable with 10 MHz ± 15%, 50% nominal, 40% or 60% worst-case, duty-cycle square waves. This output pair is activated when a collision is detected on the network, during self-test (heartbeat) as the SQE_test sequence, or after the watchdog timer has expired to indicate that the twisted-pair transmitter is disabled. This pair should be isolated from the AUI-transceiver cable by a pulse transformer, as required by 802.3.*
10,18, 28	V_{DD}	—	**5 V Power Supply.**
11	AP	I/O	**Autopolarity.** This pin is a dual-function pin which determines if the autopolarity function should be enabled. The function is enabled if the pin is HIGH and is disabled if the pin is LOW. Thus backward compatible with the earlier version, the pin is also capable of driving an LED if the function is enabled. See Figure 11 for the recommended circuit configuration. **Warning: This pin must never be connected directly to V_{DD} because of excessive power supply current flow.**
12	JLED	O	**Jabber Indicator.** Indicates watchdog timer has timed out and the twisted-pair drivers have been disabled.
13	XTAL	I	**Crystal In.** This pin is a 20 MHz, frequency-reference input for internal chip timing.
15	CLED	O	**Collision Indicator.** Indicates a collision has been detected by the TPMAU2.
16	RLED	O	**Receive Indicator.** Indicates a reception from the TP network is in progress.
17	XLED	O	**Transmit Indicator.** Indicates a transmission onto the TP network is in progress.
19—22	TPO, $\overline{\text{TPO}}$, PEC, $\overline{\text{PEC}}$	O	**Twisted-Pair Out/Pre-equalization Control.** These four outputs constitute the twisted-pair drivers with predistortion capability. The TPO/$\overline{\text{TPO}}$ outputs generate the 10 Mbits/s Manchester-encoded data. The PEC/$\overline{\text{PEC}}$ outputs mirror the TPO/$\overline{\text{TPO}}$ outputs except for fat-bit† occurrences. During the second half of a fat bit (either high or low), the PEC/$\overline{\text{PEC}}$ outputs are inverted with respect to TPO/$\overline{\text{TPO}}$ outputs. This signal behavior reduces the amount of jitter by preventing overcharge on the twisted-pair media.
26, 27	$\overline{\text{IN}}$, IN	I	**TP Receive Pair.** A differential receiver tied to the receive transformer pair of the twisted-pair wire. The receive pair of the twisted-pair medium is driven with 10 Mbits/s Manchester-encoded data.

* Please consult *Using the T7220 Twisted-Pair Medium Attachment Unit (TPMAU) without the AUI Transformer* (TN90-013SMOS) for use of this device without an AUI isolation transformer.

† Fat bit is the midbit-to-midbit time during the CD0-to-CD1 transition or CD1-to-CD0 transition, each of which is nominally 100 ns.

Overview

The T7220A device provides the transmit, receive, and collision-detection functions as specified by the IEEE 802.3 10BASE-T draft standard for use in a 10 Mbits/s CSMA/CD Ethernet on a twisted-pair LAN application. It is an equivalent of Ethernet's transceiver chip but is used as the interface to the twisted pair. Figure 3 shows a typical application example. Figures 4 and 5 show details of the circuitry. The *10BASE-T Twisted-Pair Interface Design Considerations* (TN90-012SMOS) Technical Note describes the transmit circuitry.

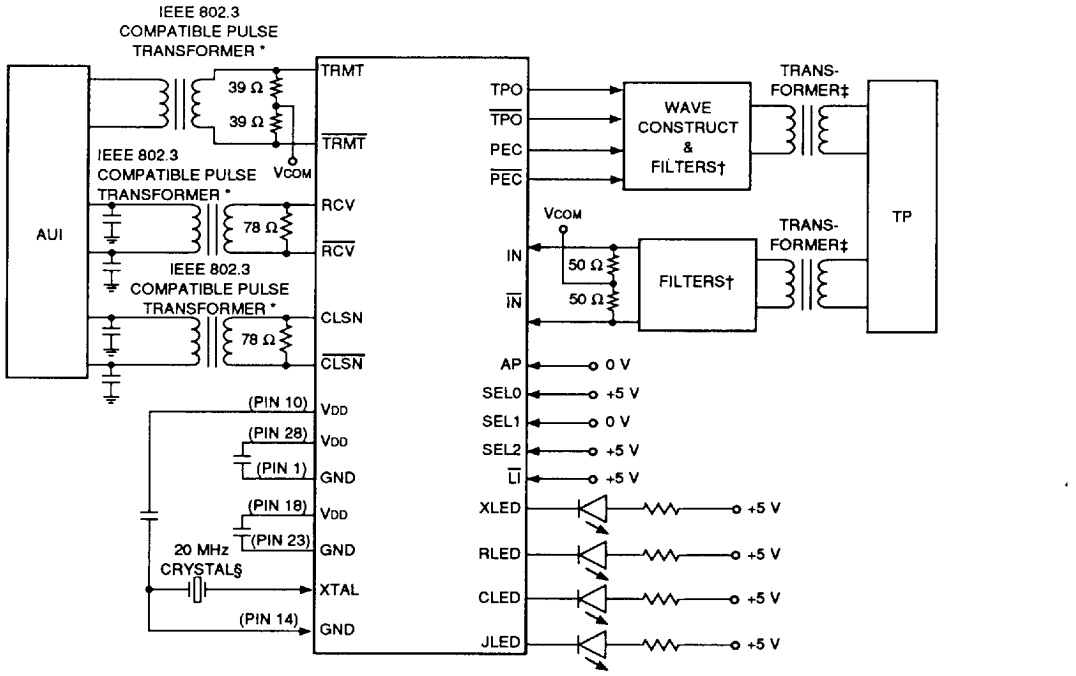
The transmit section transfers data from the AUI cable to the twisted-pair network, and the receive section transfers data from the twisted pair to the AUI. The collision-detection capability senses data being simultaneously transmitted and received. It reacts by sending a 10 MHz square wave onto the AUI-CI circuit.

Overview (continued)

In addition to these functions, there are three strapping options to select the proper mode (see Table 2). Enabling the link-integrity function causes a pulse to be transmitted in the absence of data transmission. The receiver recognizes link-integrity pulses, acknowledging that in the absence of receive traffic, the link is up. The link-integrity pin can be configured as an input or as an output. When the link-integrity pin is configured as an input, the function can be enabled or disabled. When the link-integrity pin is configured as an output, the function is enabled and the status of the link (up or down) is indicated. When the SQE_test sequence function is enabled, it allows the SQE_test sequence to be transmitted to the DTE after every successful transmission on the twisted-pair network.

The strapping options also enable the selection of two line lengths: normal or extended. When standard 10BASE-T values are implemented, normal line length is used. When the TP squelch thresholds are lowered, extended line length is used. When nonstandard 802.3 line lengths are desired, the device squelch threshold can be reduced by configuring the device properly. The device also contains an autopolarity function which can determine if the receive twisted pair has been wired with polarity reversal. If the twisted pair is wired with polarity reversal, the device automatically corrects for this error condition. Also, the autopolarity function can be used with an LED to display the status of the polarity of the receive twisted pair.

There are four drivers capable of driving four LEDs to indicate the status of the receive, transmit, collision, and jabber functions. Also, when configured correctly, two additional LEDs can display autopolarity and link-integrity status.



* Suggested transformers for the AUI interface are the TDK Corp. (TLA-100-3E), Coilcraft (LAXET304 or LO323-A), Pulse Engineering Inc. (PE64503), or equivalents.

† Possible filters are the TDK Corp. (0921ES), CTS Corp. — Knight Div. (9561928-01), Coilcraft (K9686-B), Pulse Engineering Inc. (PE32101), or equivalents.

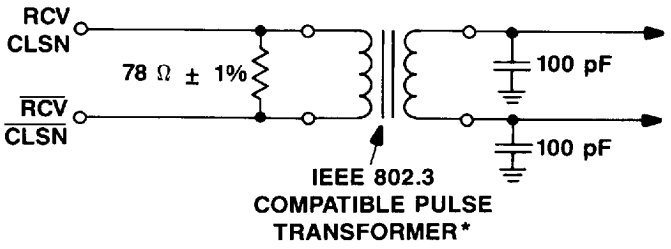
‡ Required transformers for the TP interface are the AT&T (2759A), Coilcraft (LAXIOT-200), Pulse Engineering (PE65263), or equivalents.

§ The recommended crystal is MTRON MP-1 (20 MHz).

Note: Mode 5 is shown which is backward compatible with the T7220.

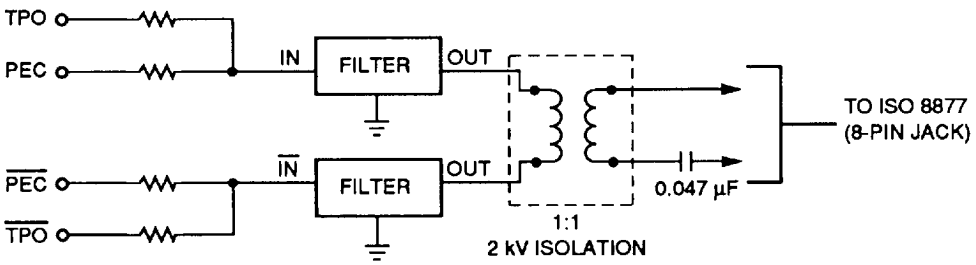
Figure 3. Typical System Configuration

Overview (continued)



* Suggested transformers are the TDK Corp. (TLA-100-3E), Coilcraft (LAXET304 or LO323-A), Pulse Engineering Inc. (PE64503), or equivalents.

Figure 4. Typical External Circuit on the Outputs of RCV/$\overline{\text{RCV}}$ and CLSN/$\overline{\text{CLSN}}$



Note: Various combinations of filters, transformers, and common-mode chokes are available in a single package from TDK Corp., CTS Corp. — Knight Div., Coilcraft, and Pulse Engineering Inc.

Figure 5. Example of Transmit Circuitry

Architecture

Transmit Path (AUI to TP)

AUI Receiver

The TPMAU2 receives transmit data from the DTE on the AUI-DO circuit as described in IEEE 802.3 on the TRMT pins and transmits this data onto a twisted-pair network. The input must be transformer-coupled to the AUI circuit (802.3 required isolation), and the receiver is able to resolve differential signals as small as 300 mV peak and as large as 1315 mV peak. dc biasing should be provided externally to the chip, with the common-mode voltage set to nominal 2.5 V.

The common-mode voltage (V_{COM} in Figure 3) should be bypassed close to the chip, so the composite common-mode signal is 2.5 V ± 50 mV.

The differential input resistance of the TRMT/$\overline{\text{TRMT}}$ pins is 20 kΩ ± 20%. The differential capacitance between the two input pins has a maximum value of 10 pF at 10 MHz.

AUI Squelch

A single-level biasing scheme is used to reject spurious noise on the TRMT/$\overline{\text{TRMT}}$ pins and prevents it from propagating onto the network. The squelch function is described in Figures 6 and 7. Figure 6 sets up the variables by showing the amplitude and duration of a differential input at pins TRMT and $\overline{\text{TRMT}}$. Figure 7 shows the regions where the part must either remain squelched or where the part must unsquelch and begin transmitting.

The transmit path will unsquelch on the first pulse of sufficient magnitude and duration, which is the first bit of a packet preamble. This first pulse can be described by an amplitude and a duration, as shown in Figure 6. It should be noted that the signal shown is the differential voltage at the TRMT, $\overline{\text{TRMT}}$ inputs. This signal is fed into a comparator, which will unsquelch the part if the input pulse meets the requirements set out in Figure 7. By cross referencing the signal pulse duration (time) and differential amplitude, a point on the graph is found. If this point is in the unsquelch region, the data path will turn on. If the point is in the shaded area, the device behavior is uncertain. The region of uncertainty allows for process variations from device to device.

Once turned off, the squelch remains off until an IDL pulse is detected or the input signal does not exceed the detection threshold for 475 ns ± 75 ns. The part is required to successfully identify all IDL pulses having a minimum length of 200 ns.

Figure 6. AUI Squelch Diagram

Architecture (continued)

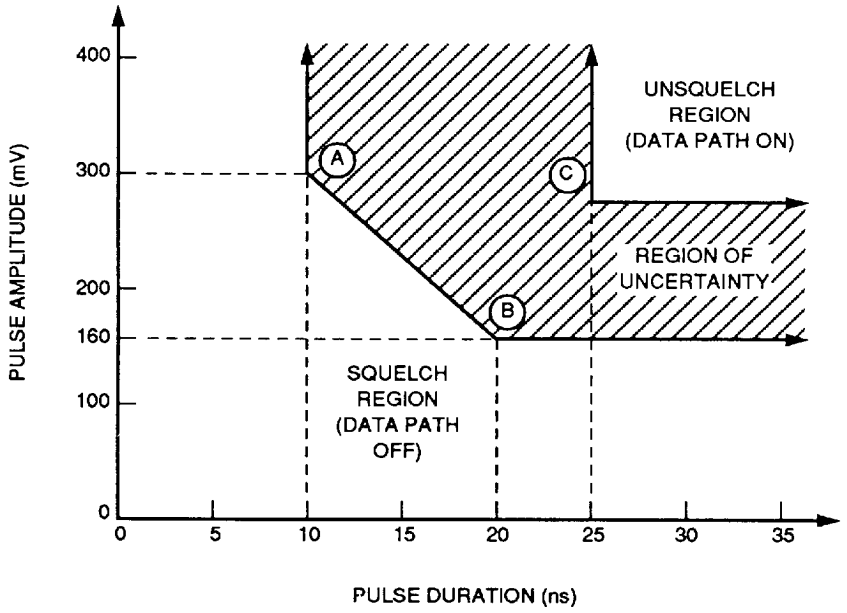


Figure 7. AUI Squelch Template

TP Predistortion

An internal, analog, delay-line is used to generate the predistortion signals at PEC and $\overline{\text{PEC}}$. The signal PEC copies TPO for the first 50 ns after each transition in TPO, then PEC inverts its output logic state. This is shown in Figure 8.

A delay lock loop, referenced to the crystal clock, is used to generate the internal delay line.

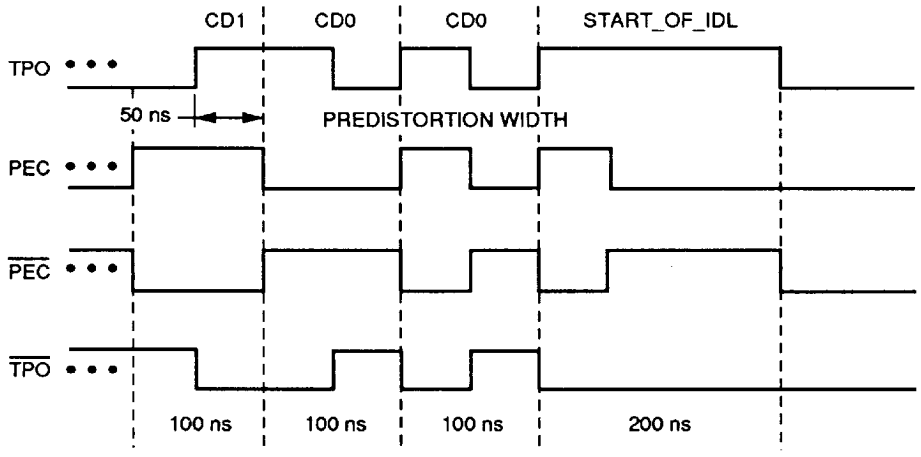


Figure 8. Timing Diagram of Transmit Predistortion

Architecture (continued)

TP Driver Characteristics

The drivers output CMOS logic levels with a source resistance of less than 10 Ω and a maximum current rating of 25 mA dc. When driving a purely capacitive load, the pins will swing from rail to rail (V_{DD} to V_{SS}).

All TP output driver pins are driven low as a result of any of the following: there is an AUI IDL pulse of at least 200 ns duration, the output driver is jabbed, the link-integrity option is enabled and there is a link failure, or an IDL pulse is not detected at the end of a packet and the input does not exceed the detection threshold for 475 ns ± 75 ns.

When the driver detects that it has finished sending an IDL pulse onto the TP, a timer of not more than 500 ns is started. While this timer is active, activity on the TRMT/$\overline{\text{TRMT}}$ inputs is ignored.

Receive Path (TP to AUI)

TP Receiver

The TP receiver is connected to a band-limiting filter, whose input is transformer-coupled to the twisted pair. The receiver is able to resolve differential signals as small as 350 mV peak. The common-mode input voltage of the input signals is required from the band-limiting filters to be nominally 2.5 V. The dc differential input impedance of the IN/$\overline{\text{IN}}$ pins is 20 kΩ ± 20%.

The common-mode voltage should be bypased close to the chip so that the composite common-mode signal is 2.5 V ± 50 mV.

TP Receiver Smart Squelch

The receiver rejects the following signals in accordance with section 14.3.1.3.2 of the 802.3 standard:

1. All signals that, when measured through the recommended input filter, produce a peak magnitude of less than 300 mV.
2. All continuous sinusoidal signals of amplitude less than 3.1 V peak and frequency less than 2 MHz.
3. All single sinusoidal cycles with amplitude less than 3.1 V peak and starting with either polarity where the frequency is between 2 MHz and 15 MHz. For a period of 4 BT before and after this single cycle, the received signal must conform to step 1 above.

AUI Driver Characteristics

This driver differentially drives a current onto the load connected between the RCV and $\overline{\text{RCV}}$ pins. The current through the load results in an output voltage between ±0.6 V and ±1.2 V measured differentially between the two pins. An external resistor (78 Ω) and capacitors (100 pF) must be connected for proper termination, as shown in Figure 4. The capacitors shown may be connected to CIRCUIT GROUND on the AUI side of the transformer. They are used to reduce the ac common-mode output voltage, and to reduce pulse overshoot caused by the leakage inductance of the pulse transformer.

The output, when properly terminated, is in accordance with IEEE 802.3 standard, Section 7.4.1 for MAUs.

When the driver detects that it has finished sending an IDL pulse onto the AUI, a timer of not more than 500 ns is started. While this timer is active, activity on the IN/$\overline{\text{IN}}$ inputs is ignored, and the AUI driver discharges the current stored in the inductive load.

Collision

The CS0 signal is placed on the AUI-CI circuit whenever a collision condition exists. A state of collision exists whenever there are valid signals being input to the TPMAU2 from the network and from the DTE simultaneously and the TPMAU2 is not in a link-failure state.

The CS0 signal is a periodic square wave at 10 MHz ± 15% with a duty cycle no worse than 40/60 or 60/40. This signal is presented to the AUI-CI circuit no more than 9 BT after the chip detects a collision. Refer to IEEE 802.3, Section 14.2.1.4.

If the receive inputs, IN/$\overline{\text{IN}}$, become active while there is activity on the transmit inputs, TRMT/$\overline{\text{TRMT}}$, the loopback data on RCV/$\overline{\text{RCV}}$ switches from transmit data to receive data. Refer to Section 14.2.1.4 of the 10BASE-T standard.

If a collision condition exits with IN/$\overline{\text{IN}}$ having gone idle while TRMT/$\overline{\text{TRMT}}$ are still active, SQE continues for 7 BT ± 2 BT. If a collision condition exits with TRMT/$\overline{\text{TRMT}}$ having gone idle while IN/$\overline{\text{IN}}$ are still active, SQE can continue for up to 9 BT.

Architecture (continued)

Collision AUI Driver

This driver has the same electrical characteristics as the AUI driver for the receive path, except as already noted regarding signal requirements.

Jabber (Watchdog Timer)

The chip contains a self-interrupt capability to inhibit transmit data from being passed onto the network from a defective DTE. The chip provides a nominal window of 50 ms, during which time a normal data link frame can be transmitted. If the frame length exceeds this duration, the chip immediately inhibits all further transmission of that frame and starts the collision-presence function by placing a CS0 signal on the AUI-CI circuit. Refer to IEEE 802.3, Section 14.2.1.6.

When activity on the AUI-DO circuit has ceased, the chip continues to present the CS0 signal to the AUI-CI circuit for 625 ms ± 125 ms. The chip then returns to the idle state. Refer to IEEE 802.3, Section 14.2.1.6.

The transmission of link-integrity pulses from the TP drivers is not inhibited if the TPMAU2 is jabbed and if the $\overline{LI}$ pin is pulled active-low.

SQE_Test (Heartbeat)

When the AUI-DO circuit has gone idle after a successful transmission of a frame to the twisted-pair network and when the proper mode is selected, the chip presents the CS0 signal to the AUI-CI circuit.

Upon the conclusion of a successful transmission onto the network media, the chip presents the CS0 signal within 11 BT ± 5 BT of the end of activity on the AUI-DO circuit. The CS0 signal is presented for 10 BT ± 5 BT (this is known as heartbeat or SQE_test sequence), after which the chip presents an IDL on the AUI-CI and returns to the idle state. Refer to IEEE 802.3, Section 14.2.1.5.

A successful transmission is defined as an uninterrupted packet transmission onto the network media. Interruption sources include jabber or link failure.

Link Integrity

The chip can determine if the receive twisted-pair link is faulty. Enabling the link-integrity function allows the RLED receive traffic indicator to display the status of the receive twisted-pair link. Also, the $\overline{LI}$ pin may itself be connected to an LED to display the status of the receive twisted-pair link. It also permits the active disabling of the transmit and loopback paths onboard the TPMAU2 chip in response to a link-integrity fault.

In the absence of receive traffic, the twisted-pair receiver on the chip can detect periodic link-integrity pulses on the receive pair. A link-integrity pulse is described as a 100 ns ± 20% HIGH signal with predistortion followed by a return to idle. The chip provides a link-integrity reception window, during which a link pulse is expected in the absence of receive traffic. The link-integrity window nominally opens 6.5 ms after the receipt of a link-integrity pulse or the end of a data frame. The window closes nominally 104 ms after the receipt of a link-integrity pulse or the end of a data frame. 10BASE-T requires that the window open with the expiration of the T_link_test_min timer, and that the window close with the expiration of the T_link_loss or T_link_test_max timer, depending on the current status of the link-integrity state machine. For the TPMAU2, the T_link_loss and T_link_test_max timers have the same nominal value. Refer to IEEE 802.3i, Section 14.2.1.7.

If a link pulse is received before the link-integrity reception window opens, it is ignored. If no link-integrity pulse is received while the link-integrity reception window is open, there is a link failure. The RLED indicator is turned off, and the chip's transmit, loopback, and receive functions are disabled. If a link-integrity pulse or receive traffic is received while the link-integrity reception window is open, the timers involved are reset, and the RLED indicator remains on or flashes, as described in the LED Status section.

Once the TPMAU2 has detected a link failure, one of two events must occur before the TPMAU2 re-enables transmission and reception of data. The first possible event is the reception of two (link_count) consecutive link-integrity pulses which must both fall within the link-integrity reception window and be separated by at least a nominal 6.5 ms. The second possible event is the reception of a data packet from the twisted pair. With either of these events, the TPMAU2 enters a wait-state and continues to disable loopback, transmit, and receive functions. This continues until the TPMAU2 determines that there is no traffic going in either the transmit or receive direction, whereupon the part enters the idle state, and the RLED indicator shows the link is present. Refer to IEEE 802.3i, Section 14.2.1.7.

Architecture (continued)

When the link-integrity function is enabled, the TPMAU2 also transmits link-integrity pulses onto the transmit twisted-pair link. In the absence of transmit traffic, a link-integrity pulse is transmitted at a nominal rate of once per 16 ms. Link-integrity pulses continue to be transmitted when the part is jabbed by the watchdog timer or there is link-integrity failure.

If the link-integrity function option is disabled, the RLED indicator remains on in the absence of receive traffic, and no link-integrity pulses are transmitted in the absence of traffic. Received link-integrity pulses are also ignored at the IN/$\overline{\text{IN}}$ inputs.

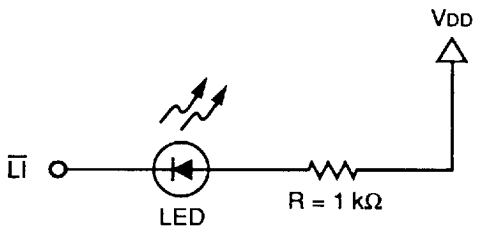
Description of $\overline{\text{LI}}$ pin interface

This dual-function pin must be configured in one of two different operating modes. As described in the Modes of Operation section, the $\overline{\text{LI}}$ pin can be either an input only or an output only pin.

When configured for the input only mode, the pin input either enables or disables the link-integrity function. If the pin is held LOW, the function is enabled. If the pin is held HIGH, or allowed to float where an internal pull-up resistor pulls it HIGH, it disables the function. The status of the link integrity function is displayed on the RLED pin when the $\overline{\text{LI}}$ pin is configured in this mode.

When the $\overline{\text{LI}}$ pin is configured in the output only mode, the pin drives LOW when the part is in a link-failure state, and when the link is up, the pin is driven HIGH. The link-integrity function is always enabled when the $\overline{\text{LI}}$ pin is configured in this mode.

These specific requirements enable the part to remain backward compatible with the earlier version of the T7220.



Note: Valid only in modes 2 and 6.

Figure 9. Diagram for LED Connection at $\overline{\text{LI}}$ Pin

Autopolarity

The device can determine if the receive twisted-pair link has been wired with a polarity reversal, and if so, the device automatically corrects for this error condition, when the function is enabled. Also, the AP pin itself can be connected to an LED to display the status of the polarity of the receive twisted-pair link.

When enabled, the device powers up the function in the up state, and determines if the receive wires are reversed. The device examines the IDL pulse at the end of each packet and uses that information to sense the polarity. If the part determines that the incoming IDL pulse is of the proper polarity, the part remains in the up state. If the part determines that the polarity of the link is reversed, it internally corrects for it, ensuring all follow-on packets are sent across the AUI with the correct polarity.

More specifically, the behavior of the autopolarity function is governed by the state diagram shown in Figure 10. The part powers up in the up state, where the polarities required are as governed by the 802.3. While in this state, the part looks at each of the two polarity events. The first is the polarity of the IDL pulse at the trailing edge of each data frame. The second polarity event is a link-integrity pulse, provided the link-integrity function has been enabled. If the part is in a given state, up for example, and a polarity event, say an IDL pulse, comes in up_side_down, the part moves into a count state, where it requires three more polarity events, in this case down. If a correct polarity event, say a link pulse, arrives while the part is counting opposite polarity events, the part is restored to the up state, and the counter is reset to 0.

The AP pin can drive an LED to indicate the status of the autopolarity function. For backward compatibility with earlier versions, a strobing technique is used. The part lets the pin float, and senses the input. If the user has the pin connected to ground, the function is disabled. If the user has the pin connected to V_{DD} through an LED, the function is enabled. Once the decision on whether the function is active or not has been made, the pin is allowed to float HIGH if the function is enabled and the receive polarity is correct, thus keeping the LED off. If the function is enabled and the receive polarity is determined to be reversed, the pin is driven LOW to light the LED. The sampling process to determine the status of the autopolarity function (enable or disable) occurs approximately every 26 ms and lasts for approximately 1 μs; thus it does not affect the visual appearance of the LED, should it be lit.

Architecture (continued)

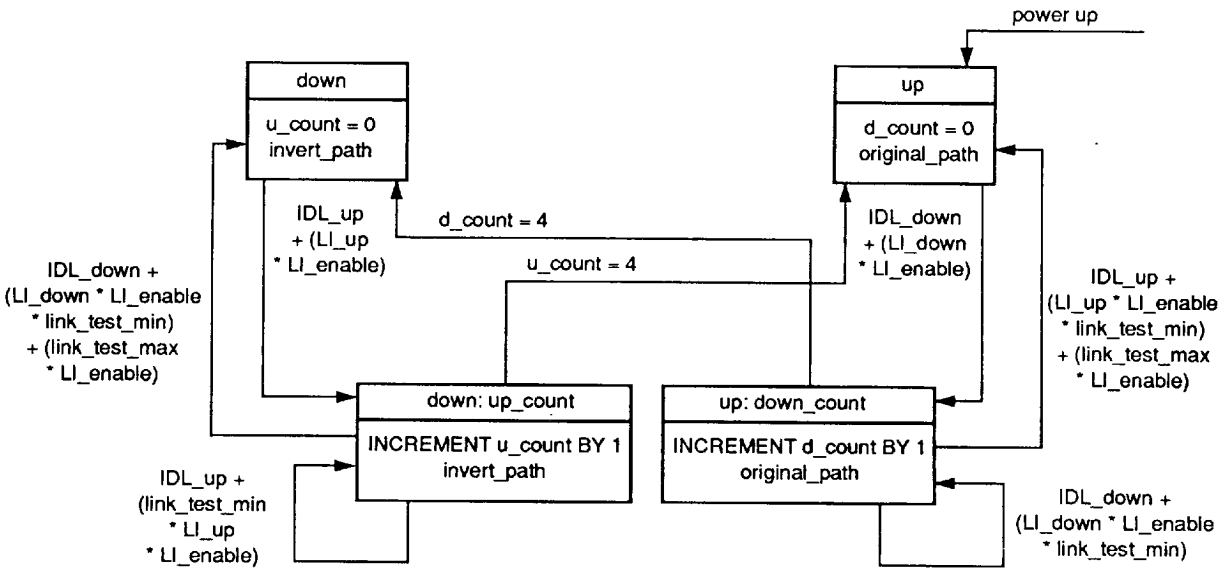


Figure 10. Autopolarity State Diagram

Warning: The AP pin should never be connected directly to V_{DD}. A minimum of 1 kΩ of series resistance is required.

Figure 11 illustrates how the LED should be connected.

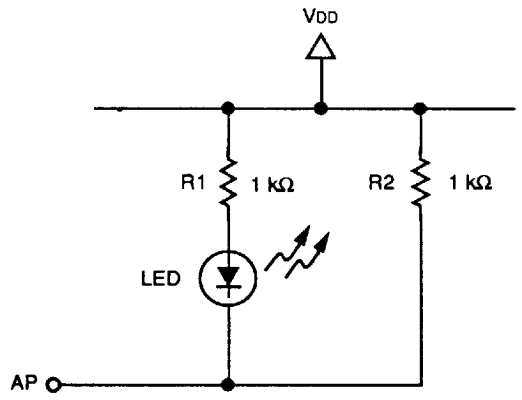


Figure 11. Connection of LED to AP Pin (Autopolarity Function Enabled)

Architecture (continued)

Modes of Operation

The select pins are decoded to provide one of eight modes of operation. These modes are summarized in the Table 2.

Table 2. Mode Description

Mode	SEL0(4)	SEL1(25)	SEL2(24)	Mode Description
0	0	0	0	No heartbeat, normal timing, extended line length, $\overline{LI}$ input only
1	0	0	1	No heartbeat, normal timing, normal line length, $\overline{LI}$ input only
2	0	1	0	No heartbeat, normal timing, normal line length, $\overline{LI}$ output only
3	0	1	1	dc test mode
4	1	0	0	Yes heartbeat, normal timing, extended line length, $\overline{LI}$ input only
5	1	0	1	Yes heartbeat, normal timing, normal line length, $\overline{LI}$ input only
6	1	1	0	Yes heartbeat, normal timing, normal line length, $\overline{LI}$ output only
7	1	1	1	ac test mode, yes heartbeat, normal line length, $\overline{LI}$ output only

The following list describes each of the statements in the Mode Description column of Table 2.

- **Yes/No Heartbeat**. Yes heartbeat means that the SQE_test or heartbeat function, as described elsewhere, is enabled; no heartbeat means the heartbeat function is disabled as required for when the MAU is connected to a repeater.
- **Normal/Extended Line Length**. This indicates if the TP squelch thresholds have been lowered for use with extended line lengths, or if the standard 10BASE-T values (normal) are in use.
- **$\overline{LI}$ Input/Output**. The $\overline{LI}$ pin can be configured to be an input pin, whereby the link-integrity function can be enabled or disabled. The $\overline{LI}$ pin can also be configured as an output pin to indicate the status of the link (up or down). If the $\overline{LI}$ pin is configured as an output, the link-integrity function is enabled.
- **ac/dc Test Modes**. The device can be configured in test modes to enhance production testing of the device.

Test Modes

The T7220A TPMAU2 has two internal test modes, labeled ac and dc. In a global sense, the ac test mode speeds up some internal timers, so that events happen in a shorter amount of time. For instance, the jabber would jab transmission after only 50 μs instead of 50 ms. This is done to reduce production test time. Similarly, the dc test mode allows examination of the oscillator behavior and the output resistance of the TP and LED outputs. Also, dc test mode allows a quick examination of the current provided by both AUI output current drivers. A 39 Ω resistor should be connected between the output pins during measurement of this current.

The part is placed into either of the test modes by proper selection of the mode select pins, as described in the previous paragraphs.

Architecture (continued)

LED Status

Four LEDs provide the user with a visual indication of the status and operation of the MAU. The TPMAU2 provides the logic signals to drive the LEDs.

XLED

The following XLED values (on or off) indicate transmission status:

- The LED is normally on. This indicates there is no transmission in progress.
- The LED is turned off when a valid packet is transmitted and remains off for a duration of fixed off-time (100 ms ± 10 ms), after which the LED is turned back on.
- The LED remains on for a duration of at least a minimum on-time (6 ms ± 2 ms), until it is turned off, if and when the next packet is transmitted.

RLED

The following RLED values indicate the status of reception from the twisted pair.

When $\overline{LI}$ is disabled:

- The LED is normally on, indicating there is no current receive traffic.
- The LED is turned off when a valid packet is received and remains off for a duration of fixed off-time (100 ms ± 10 ms), after which the LED is turned back on.
- The LED remains on for a duration of a minimum on-time (6 ms ± 2 ms), until it is turned off, if and when the next packet is received.

When $\overline{LI}$ is enabled:

- The LED is normally on. This indicates no receive traffic and successful reception of the link-integrity pulse.
- The LED turns off if the TPMAU2 determines there is a link failure, as previously described. This visually indicates that the link is down. The LED remains off until a link-integrity pulse or receive traffic is successfully detected, after which the LED is turned on with a minimum on-time of 1 second ± 50%.
- If the link is up, the LED can also be turned off when a valid data packet is received from the twisted pair. When a packet is received, the LED is turned off for a duration of fixed off-time (100 ms ± 10 ms), after which the LED is turned back on.
- The LED remains on for a minimum on-time (6 ms ± 2 ms), after which it is turned off when the next packet is received.

CLED

The following CLED values indicate collision status:

- The LED is normally off, indicating no collision.
- The LED is turned on when a collision is detected. It remains on for a nominal on-time of 15 ms ± 5 ms, after which it is turned back off.
- The LED is turned back on immediately upon detection of another collision. There is no minimum off-time.
- If a collision occurs while the LED is lit from a previous collision, the LED remains on for the nominal on-time following the last collision detection.

JLED

The following JLED values indicate jabbing status:

- The LED is normally off, indicating a no-jab condition.
- The LED is turned on when the watchdog timer jabs the twisted-pair network drivers. It remains on while the chip continues to jab the TP drivers.
- The LED is turned off after the watchdog timer counts out the 625 ms ± 125 ms reset time and stops jabbing the TP drivers.

Architecture (continued)

Description of LED Pin Interface

The J, X, R, and C LED drivers require an external resistor in series with the LED, which is in turn connected to V_{DD}. The driver pulls the pin LOW to turn the LED on and can sink up to 15 mA of drive current from the resistor with an output resistance of less than 50 Ω.

The $\overline{LI}$ pin (when output only) LED driver requires an external resistor in series with the LED, which is in turn connected to V_{DD}. The electrical characteristics of the driver are identical to the other LED drivers described in the previous paragraph.

Lamp Test

The RLED and XLED output drivers are normally LOW, turning the LED on. Also, the JLED and CLED output drivers are normally HIGH, turning the associated LED off. During powerup, these outputs are driven LOW for the purposes of providing a lamp test for the attached LEDs. The duration of the lamp test is 1 second ± 50%.

If the device is powered up with the link-integrity pin selected as an output only, a lamp test of 1 second ± 50% is provided. The output of the $\overline{LI}$ pin is LOW during the lamp test.

If the device is powered up with the autopolarity function enabled, the AP pin is driven LOW for 1 second ± 50% for the purposes of providing a lamp test.

The lamp test for the AP pin may be delayed from the others by up to 60 ms to allow the AP input/output buffer to be clocked into the proper state.

Crystal Oscillator

A 20 MHz, parallel-resonant crystal (100 ppm recommended) is required to control the TPMAU2's crystal oscillator. The oscillator is designed to operate with a quartz crystal with a series resistance of 25 Ω maximum and an expected crystal load of 20 pF. With this crystal, the total external capacitance, including crystal shunt capacitance C0, should not be more than 10 pF. This requires placing the crystal adjacent to the TPMAU2. The crystal shunt capacitance (C0) should not exceed 5 pF.

The crystal is connected between the XTAL pin and the adjacent GND pin on the TPMAU2.

Crystal Parameters

The following are parameters for the crystal:

- AT cut, parallel resonance with 20 pF load
- 20.000 MHz (100 ppm recommended)
- Series resistance 25 Ω maximum
- C0 shunt/holder capacitance 5 pF maximum

Board Layout Considerations (Crystal Only)

The following are board layout considerations for the crystal:

- The crystal should be located as close as physically possible to the device to minimize parasitic capacitances on the XTAL pin. Also for this reason, the device should not be socketed. The oscillator is **extremely** sensitive to any capacitance in parallel with the crystal. Too much parasitic capacitance may prevent the oscillator start-up when other anticipated worst-case conditions are present.
- Bypass capacitors are required. Please refer to the Power Considerations section.
- The device must be powered up in a normal mode of operation (modes 0, 1, 2, 4, 5, and 6 in Table 2). If operation in modes 3 or 7 is required for testing/manufacturing purposes, the device must be powered up in a normal mode, and then switched into one of the test modes.

Using an External Clock Source

An external MOS-level clock can be applied to the crystal oscillator input. In order for guaranteed operation, this clock should have at least a 45/55 duty cycle. A resistor should be added in series with the clock source to limit the amplitude of the voltage swing seen by the pin. A 500 Ω resistor works well in most cases.

If users are concerned about the duty-cycle variation caused by driving the TPMAU2 with a clock source, the following test can be done on the bench to empirically determine the best resistor value for the user's application:

- Power up the device in a normal mode, and then place the part in dc test mode, as described in the Test Modes section of this document.
- Attach an oscilloscope to the JLED pin. This pin outputs the internal clock source.
- Alter the resistor value to obtain an optimal duty-cycle ratio. Experiments have shown that a 500 Ω resistor works well for LS TTL logic levels; CMOS logic levels may need a 1 kΩ resistor.

Architecture (continued)

Warning: Under no circumstances should the clock be driven straight into the TPMAU2. Also, under no circumstances should the clock stop, not even briefly, once power is applied to the TPMAU2. If the clock to the TPMAU2 is stopped, power to the TPMAU2 must be removed, resetting the device to ensure proper behavior of the TPMAU2.

Strapping Options

All strapping options are connected to internal pull-up resistors (nominally 100 kΩ). A resistor tying a strapping option low must be able to sink 70 μA.

Power Considerations

There are six power connections to the TPMAU. There are three pairs of V_{DD} and GND connections. Table 3 describes which internal circuits are powered by each V_{DD}/GND pair.

Table 3. Power Connections

Pins	Circuits
1, 28	Analog Supplies: Analog signal receivers Energy-detection circuits Delay lock loop Band gap reference
10, 14	AUI Output Drivers: Digital polycells XTAL oscillator LED drivers
18, 23	TP CMOS Output Drivers Only

It is recommended that each pair of power supplies be bypassed with separate capacitors. Also, the bypass capacitor (1 μF recommended) for each pair should be located adjacent to the device to minimize lead inductance. All three ground pins should be connected directly to the ground plane of the board.

Reset/Powerup

The TPMAU2-IC unit is reset on powerup.

When the chip is powered up, it enters the idle state through a powerup circuit. This circuit will force all counters and internal activity lines to an inactive state, with all receivers and transmitters in an off or unbiased condition. The device does accept a powerup ramp on V_{DD} from as fast as 1 V/ms to as slow as 1 V/20 ms.

The device has a powerdown glitch protection circuit. This circuit completely resets the device, regardless of current activity, if the supply drops below 3.8 V. The device will not be re-enabled until V_{DD} exceeds 4.3 V.

The device should never be supplied with a power supply voltage other than 5 V. The device can exhibit undetermined behavior if a lower value of V_{DD} (e.g., 3.3 V) is applied to the device and sustained for a period of time. The powerdown protection is intended for protection against spikes in the power supply voltage, and not for use as a powerdown mode.

Warning: As described previously in the Modes of Operation section, the device has different test modes. Under no circumstances is the device to be powered up in any of these test modes. Device behavior is not guaranteed unless powerup occurs with the chip in a normal mode.

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Ambient Operating Temperature Range	T_A	0	70	°C
Storage Temperature Range	T_{stg}	−40	+125	°C
Power Dissipation	PD	—	720	mW
Voltage on Any Pin with Respect to Ground*	—	−0.5	V_{DD} + 0.5	V

* Except as described elsewhere in the data sheet.

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. AT&T employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and therefore can be used for comparison purposes. The HBM ESD threshold presented here is obtained by using these circuit parameters.

Table 4. ESD Threshold Voltage

Device	Voltage
T7220A-PC	TBD
T7220A-EC	TBD

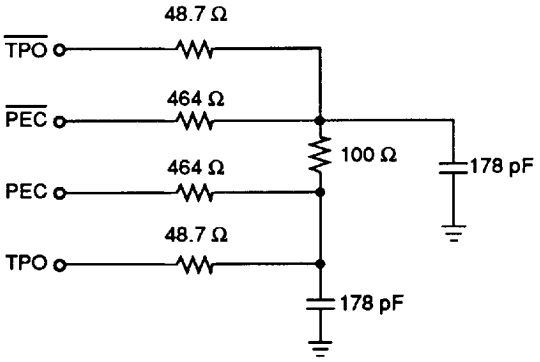
Electrical Characteristics

T_A = 0 °C to 70 °C, V_{DD} = 5 V ± 10%, V_{SS} = 0.0 V

Parameter	Symbol	Test Conditions	Min	Typ*	Max	Unit
TP Input Voltage:						
AUI	V_{IDF}	—	.300	—	1.3	V_{DIFF}
TP	V_{IDF}	—	.350	—	2.0†	V_{DIFF}
Strapping Options Input Voltage:						
Low	V_{IL}	—	—	—	0.4	V
High	V_{IH}	—	2.4	—	—	V
TP Output Voltage — TPO/$\overline{\text{TPO}}$/PEC/$\overline{\text{PEC}}$:						
Low	V_{OL}	V_{DD} = 5.0 V	—	—	0.1	V
High	V_{OH}	R_{LOAD} = 500 Ω	4.9	—	—	V
LED Drivers Output Voltage:						
Low	V_{OL}	R_{LOAD} = 2000 Ω	—	—	0.130	V
High	V_{OH}	—	4.87	—	—	V
Power Supply Voltage	—	—	4.5	—	5.5	V
Power Supply Current:						
No Traffic Load	I_{DD}	V_{DD} = 5.0 V	—	—	100	mA
With Traffic Load	I_{DD}	V_{DD} = 5.0 V	—	—	145	mA
Power Dissipation:						
No Traffic Load	PD	V_{DD} = 5.0 V	—	—	500	mW
With Traffic Load	PD	V_{DD} = 5.0 V	—	—	720	mW
AUI Output Current (Active)	I_{AVEC}	—	18	—	24	mA
AUI Output Common-Mode Voltage	—	—	—	4.0	—	V
dc Output Series Impedance:		V_{DD} = 4.5 V				
TP Drivers	Rs	I = 25 mA max	—	—	10	Ω
LED Drivers	Rs	I = 10 mA max	—	—	50	Ω
Oscillator Characteristics — Frequency	fosc	—	19.5	—	21.5	MHz
Output Rise and Fall Time:		Measured at 20% and 80% points				
TPO/$\overline{\text{TPO}}$/PEC/$\overline{\text{PEC}}$	t_r	See Figure 12.	2	—	8	ns
	t_f	See Figure 12.	2	—	8	ns
RCV/$\overline{\text{RCV}}$	t_r	See Figure 13.	3	—	9	ns
	t_f	See Figure 13.	3	—	9	ns
Receiver Differential Input Resistance	—	—	—	20	—	kΩ
Receiver Differential Input Capacitance	—	—	—	—	10	pF‡
Receiver Common-Mode Input Resistance	—	—	20	—	—	kΩ
Receiver Common-Mode Input Capacitance	—	—	—	—	20	pF‡

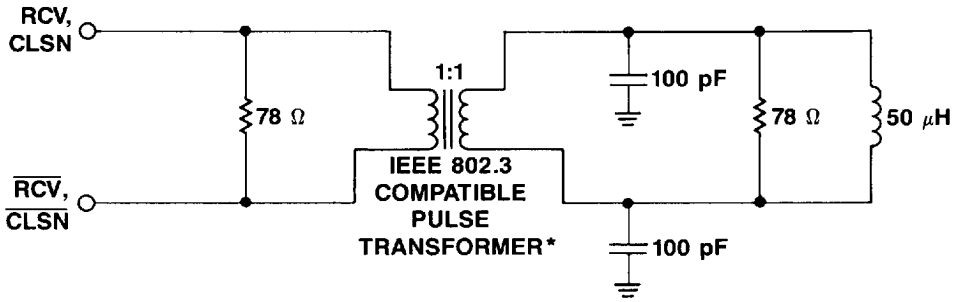
* Typical parameters are provided for design aid only. They are not guaranteed and are not subject to production testing.
† Exceeding this value may impact the jitter margin (add 2 ns of jitter), but it will not damage the device.
‡ All capacitance specifications are valid for an input frequency of 10 MHz only and are not subject to production testing.

Electrical Characteristics (continued)



Note: The resistor and capacitor values are used for testing purposes only.

Figure 12. Test Condition Load for Measurement of TP Output Drivers' Rise and Fall Times



* Required transformers are TDK Corp. (TLA-100-3E), Coilcraft (LAXET304 or LO323-A), Pulse Engineering Inc. (PE64503), or equivalents.

Figure 13. Test Condition Load for Measurement of AUI Driver's Rise and Fall Times

Timing Characteristics

Measurements are from 50% point unless otherwise noted.

Table 5. Transmit and Receive General Timing

Symbol	Parameter	Min	Max	Unit	Figure
tINVRCV	Receive Start-up Delay Time	0	500	ns	14
tTRVTPV	Transmit Start-up Delay Time	0	200	ns	15
tTRVRCV	Loopback Start-up Delay Time	0	500	ns	15
tTPVTPZ	IDL Duration Test	250	350	ns	16

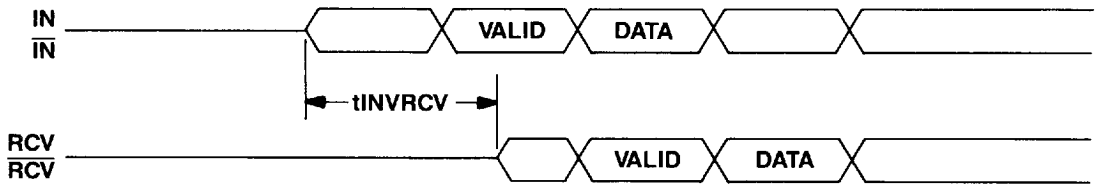


Figure 14. Receive General Timing

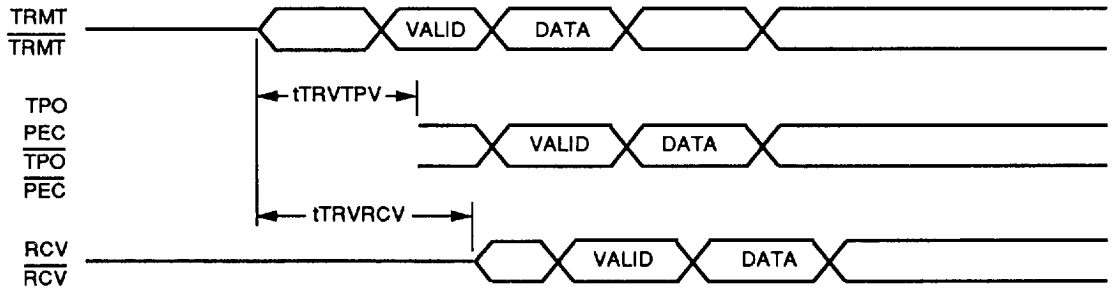
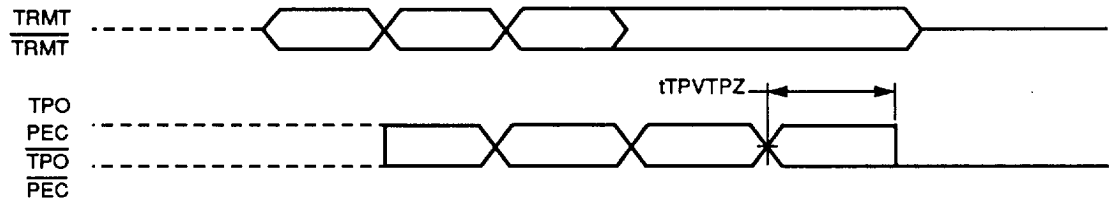


Figure 15. Transmit General Timing



Note: The AUI interface must accept very long IDL pulses on TRMT/$\overline{\text{TRMT}}$, and these pulses must be truncated to proper length before being introduced onto the TP network.

Figure 16. IDL Duration

Timing Characteristics (continued)

Table 6. Collision Timing

Symbol	Parameter	Min	Max	Unit	Figure
tINVCLV	Arrival of Data at the IN/$\overline{\text{IN}}$ Input with the Other Path Already Active to the Appearance of CS0 Signal on CLSN/$\overline{\text{CLSN}}$	0	900	ns	17
tINVRCV	Time for the Chip to Switch from Loopback of the Input Data (TRMT/$\overline{\text{TRMT}}$) at the Outputs RCV/$\overline{\text{RCV}}$ to Receive Data from IN/$\overline{\text{IN}}$	—	900	ns	17
tTRVCLV	Arrival of Data at the TRMT/$\overline{\text{TRMT}}$ Input with the Other Path Already Active to the Appearance of CS0 Signal on CLSN/$\overline{\text{CLSN}}$	0	900	ns	18
tINZCLZ	Time that SQE Continues after IN/$\overline{\text{IN}}$ Have Gone Idle, Given TRMT/$\overline{\text{TRMT}}$ Are Still Active	—	900	ns	19
tTRZCLZ	Time that SQE Continues after TRMT/$\overline{\text{TRMT}}$ Have Gone Idle, Given IN/$\overline{\text{IN}}$ Are Still Active	0	900	ns	20
tCLHCLL	CS0 High Pulse Width	40	60	ns	21
tCLLCLH	CS0 Low Pulse Width	40	60	ns	21
tCLHCLH	CS0 Frequency	8.5	11.5	MHz	21

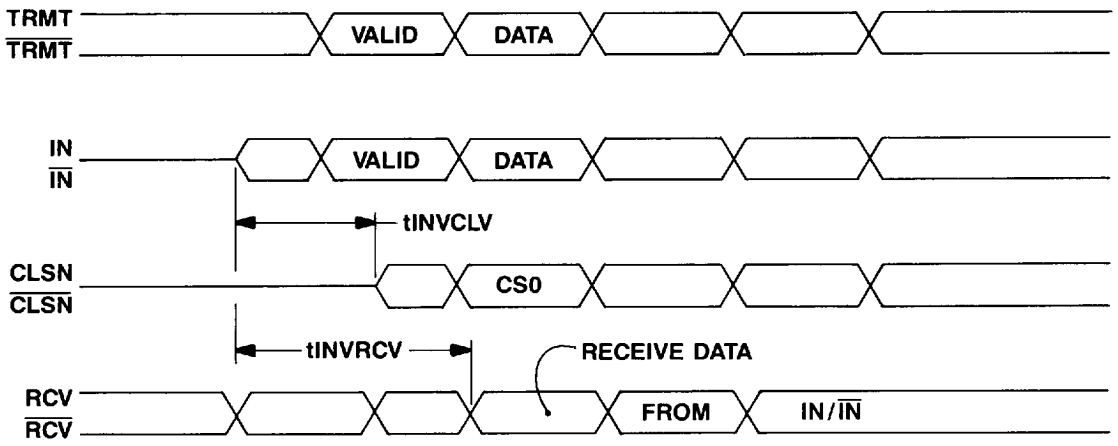


Figure 17. Collision Timing (Entry during Transmit)

Timing Characteristics (continued)

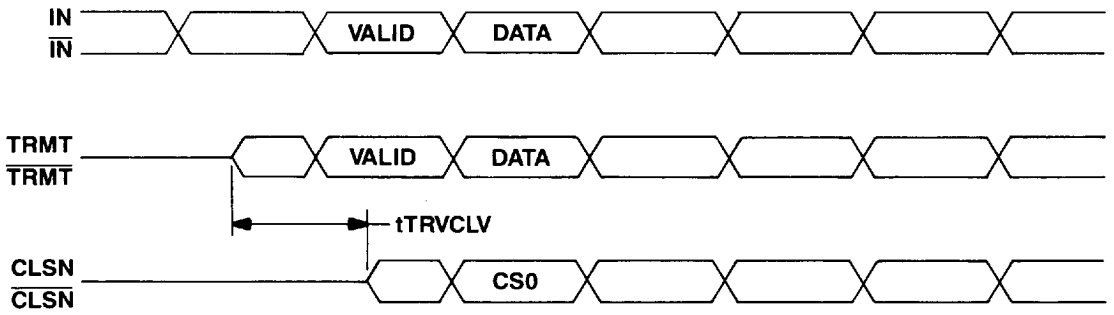


Figure 18. Collision Timing (Entry during Receive)

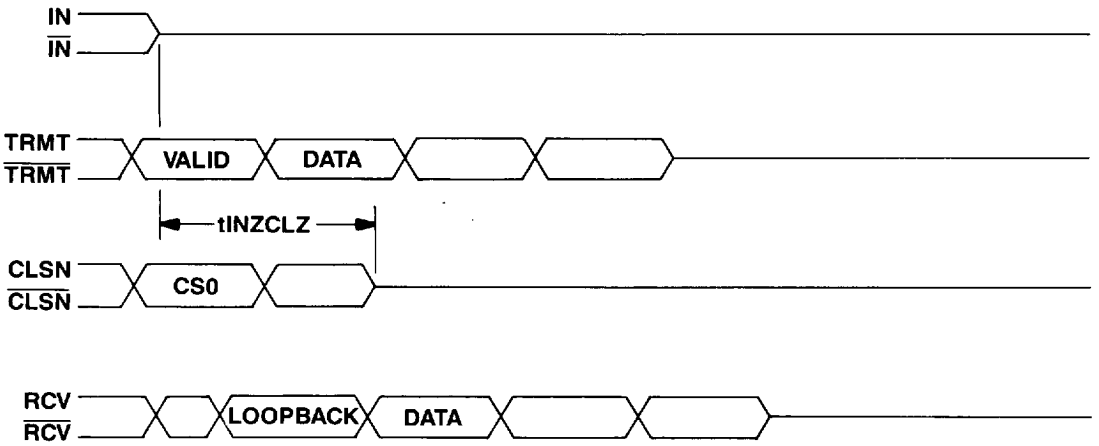


Figure 19. Collision Timing (Transmit Exit)

Timing Characteristics (continued)

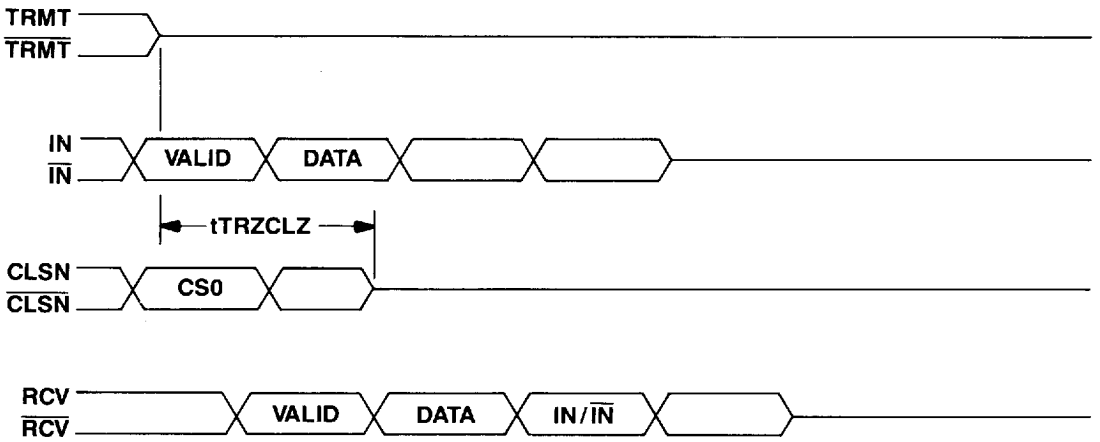


Figure 20. Collision Timing (Receive Exit)

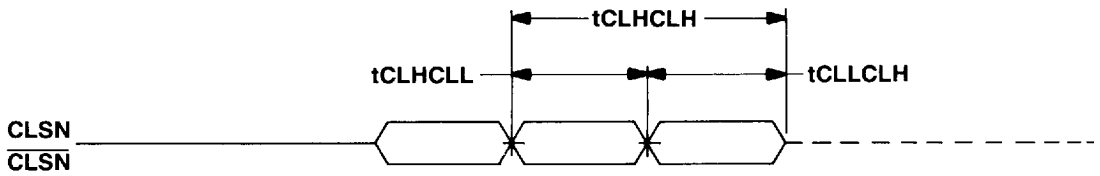


Figure 21. CS0 Characterization

Timing Characteristics (continued)

Table 7. Jabber Timing (See Figure 22.)

Symbol	Parameter	Min	Max	Unit
tTRVTPX	Assertion of Valid Data at TRMT/$\overline{\text{TRMT}}$ to the Removal of Data at the Outputs TPO/$\overline{\text{TPO}}$/PEC/$\overline{\text{PEC}}$	45	55	ms
tTPXCLV	Time from the Jabbing of the TP Outputs TPO/$\overline{\text{TPO}}$/ PEC/$\overline{\text{PEC}}$ to the Appearance of a Valid CS0 Signal on CLSN/$\overline{\text{CLSN}}$	0	900	ns
tTRZCLZ	Time from the End of Activity on TRMT/$\overline{\text{TRMT}}$ to the Removal of the CS0 Signal on CLSN/$\overline{\text{CLSN}}$	500	750	ms

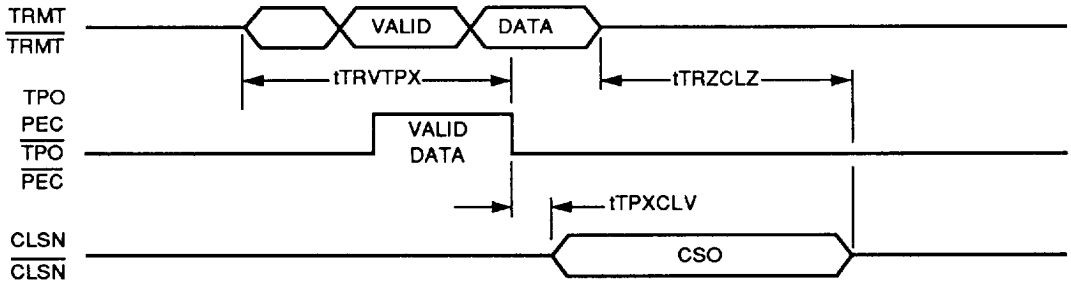


Figure 22. Jabber Timing

Table 8. Link-Integrity Pulse (See Figure 23.)

Symbol	Parameter	Min	Max	Unit
tTPLTPH	Time between Consecutive Transmitted Link-integrity Pulses	8	24	ms
tTPHTPL	Width of TPO for Link-Integrity Pulse	80	120	ns
tPEHPEL, tPBHPBL	Width of PEC for Link-Integrity Pulse	40	60	ns
$t_{SKEW(TPO-PEC)}$	Skew between Rising Edge of TPO and Rising Edge of PEC during Link Pulse Transmission	—	±10	ns
$t_{SKEW(PEC-\overline{PEC})}$	Skew between Falling Edge of PEC and Rising Edge of $\overline{\text{PEC}}$ during Link Pulse Transmission	—	±10	ns
$t_{SKEW(TPO-\overline{PEC})}$	Skew between Falling Edge of TPO and Falling Edge of $\overline{\text{PEC}}$ during Link Pulse Transmission	—	±10	ns

Timing Characteristics (continued)

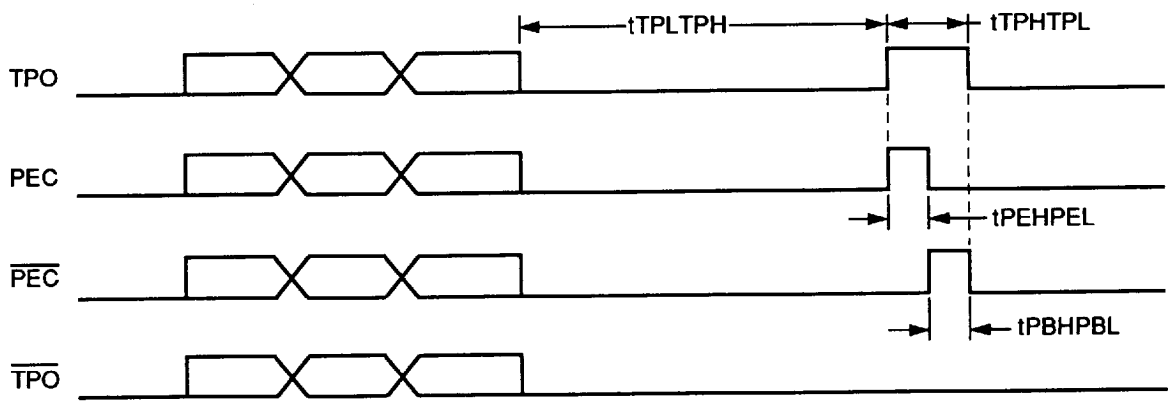


Figure 23. Transmitted Link-Integrity Pulses, $\overline{LI}$ Enabled

Table 9. Heartbeat Timing (See Figure 24.)

Symbol	Parameter	Min	Max	Unit
tTRVHBH	Setup Time for Heartbeat Strapping Option	—	10	μs
tTRZCLV	Time from the End of the IDL in the Transmit Path to the Assertion of the CS0 Heartbeat Signal on CLSN/$\overline{CLSN}$	600	1600	ns
tCLVCLZ	Time a Valid CS0 Signal, Not Including the Trailing IDL, Is Present on the CLSN/$\overline{CLSN}$ Pins	500	1500	ns

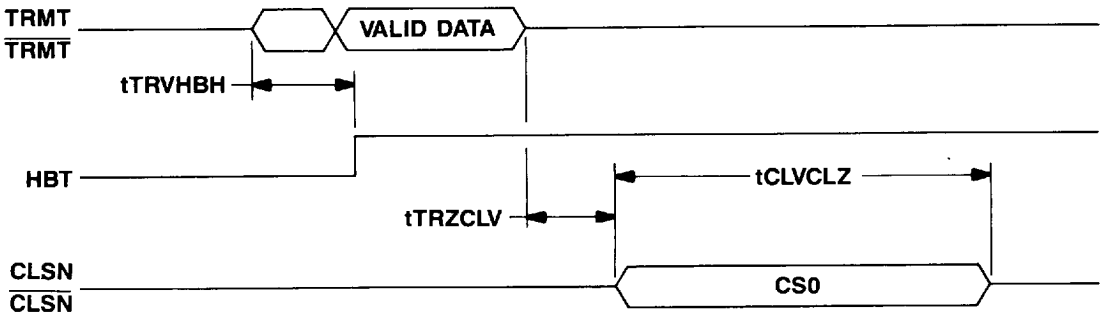


Figure 24. Heartbeat Timing

Timing Characteristics (continued)

Table 10. LED Timing

Symbol	Parameter	Min	Max	Unit	Figure
tRLHRLL	RLED Fixed Off-time	90	110	ms	25
tRLLRLH	RLED Minimum On-time	4	8	ms	25
tRLL1RLH1	RLED — Time at Which the LED Turns Off, Given that $\overline{LI}$ Is Enabled and an Absence of Receive Traffic and Link-integrity Pulses Appear	50	150	ms	26
tRLH1RLL2	RLED — Time that the LED Is Off, Given that $\overline{LI}$ Is Enabled, Until Receive Traffic or Link-integrity Pulses Appear	—	—	—	26
tRLL2RLH2	RLED — With $\overline{LI}$ Enabled, Minimum On-Time after Receive Traffic or Link-integrity Pulses Appear	500	1500	ms	26
tTRVXLH	XLED — Time to Turn Off	—	10	μs	27
tXLHXLL	XLED — Fixed Off-time	90	110	ms	27
tXLLXLH	XLED — Minimum On-time	4	8	ms	27
tINVCDL	CLED — Time to Turn On	—	10	μs	28
tCDLCDH	CLED — Nominal On-time	10	20	ms	28
tTPXJLL	JLED — Time to Turn On	—	10	μs	29
tJLLJLH	JLED — On-time While TP Drivers Are Jabbed	—	—	—	29

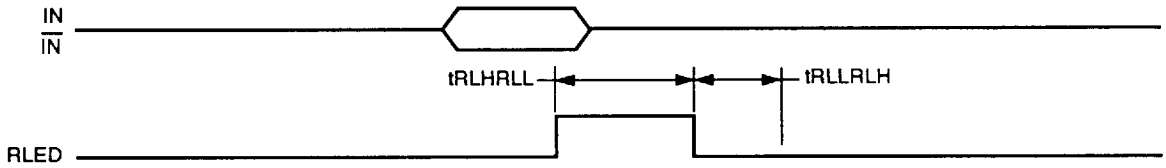


Figure 25. RLED Timing When Traffic Arrives, $\overline{LI}$ Disabled and Enabled

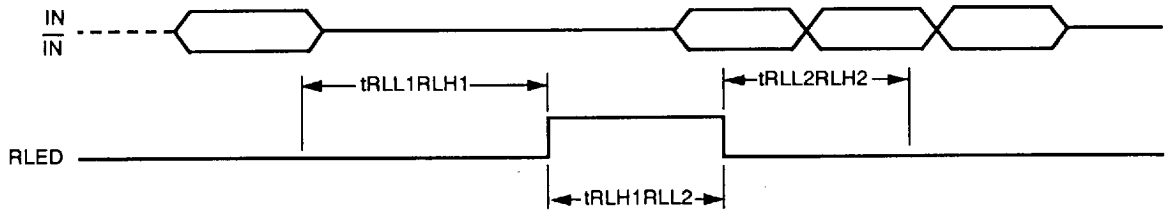


Figure 26. RLED Timing, $\overline{LI}$ Enabled

Timing Characteristics (continued)

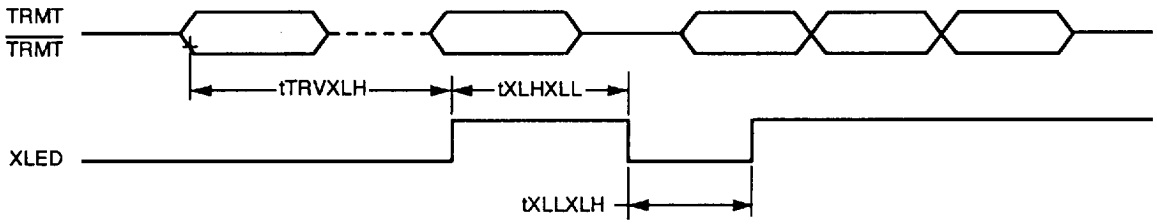


Figure 27. XLED Timing

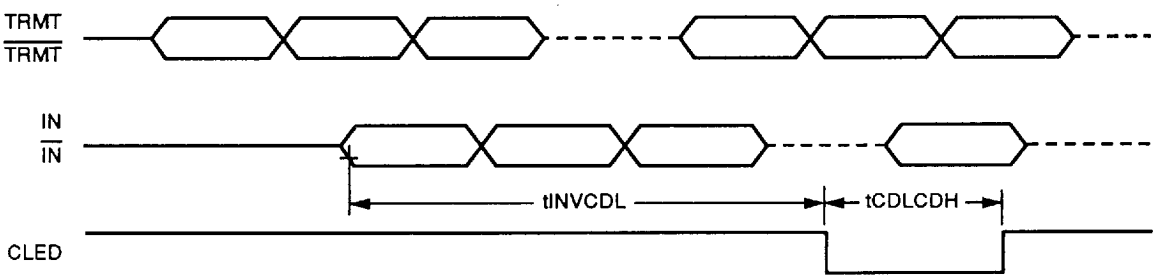


Figure 28. CLED Timing

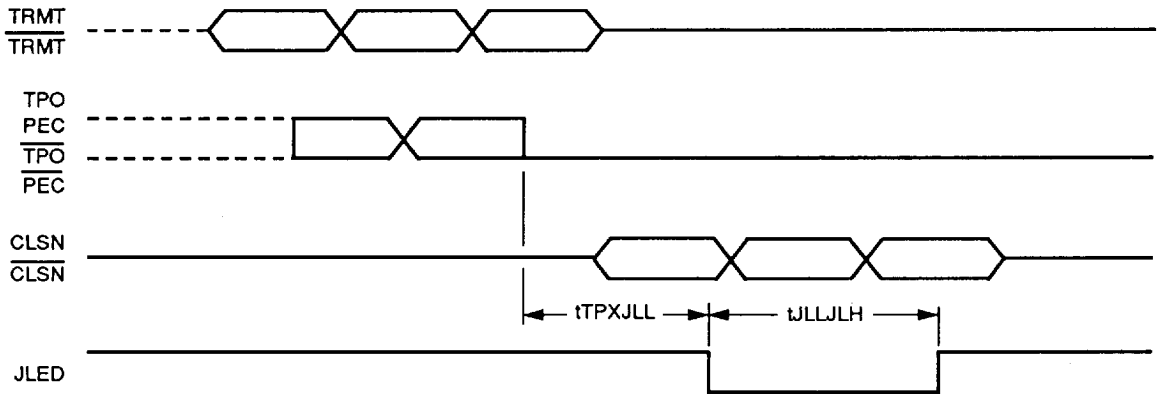
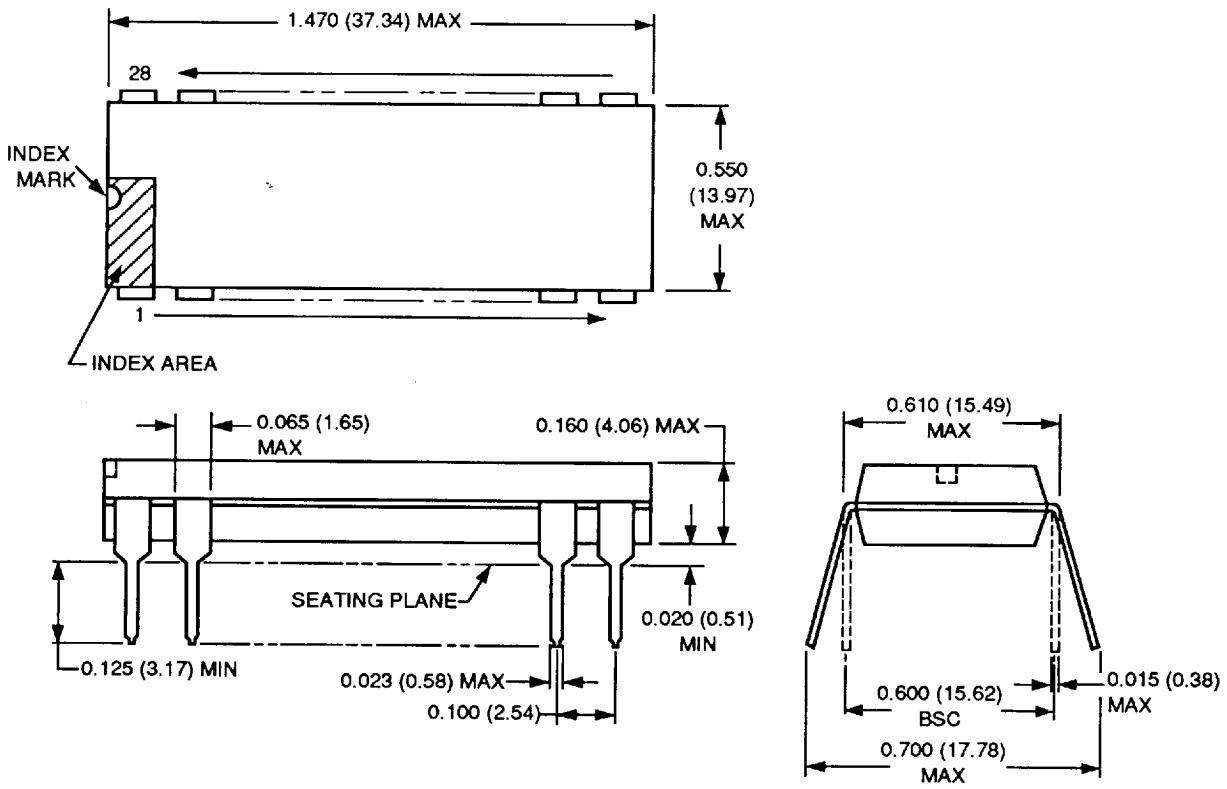


Figure 29. JLED Timing

Outline Diagrams

28-Pin, Plastic DIP

Dimensions are in inches and (millimeters).



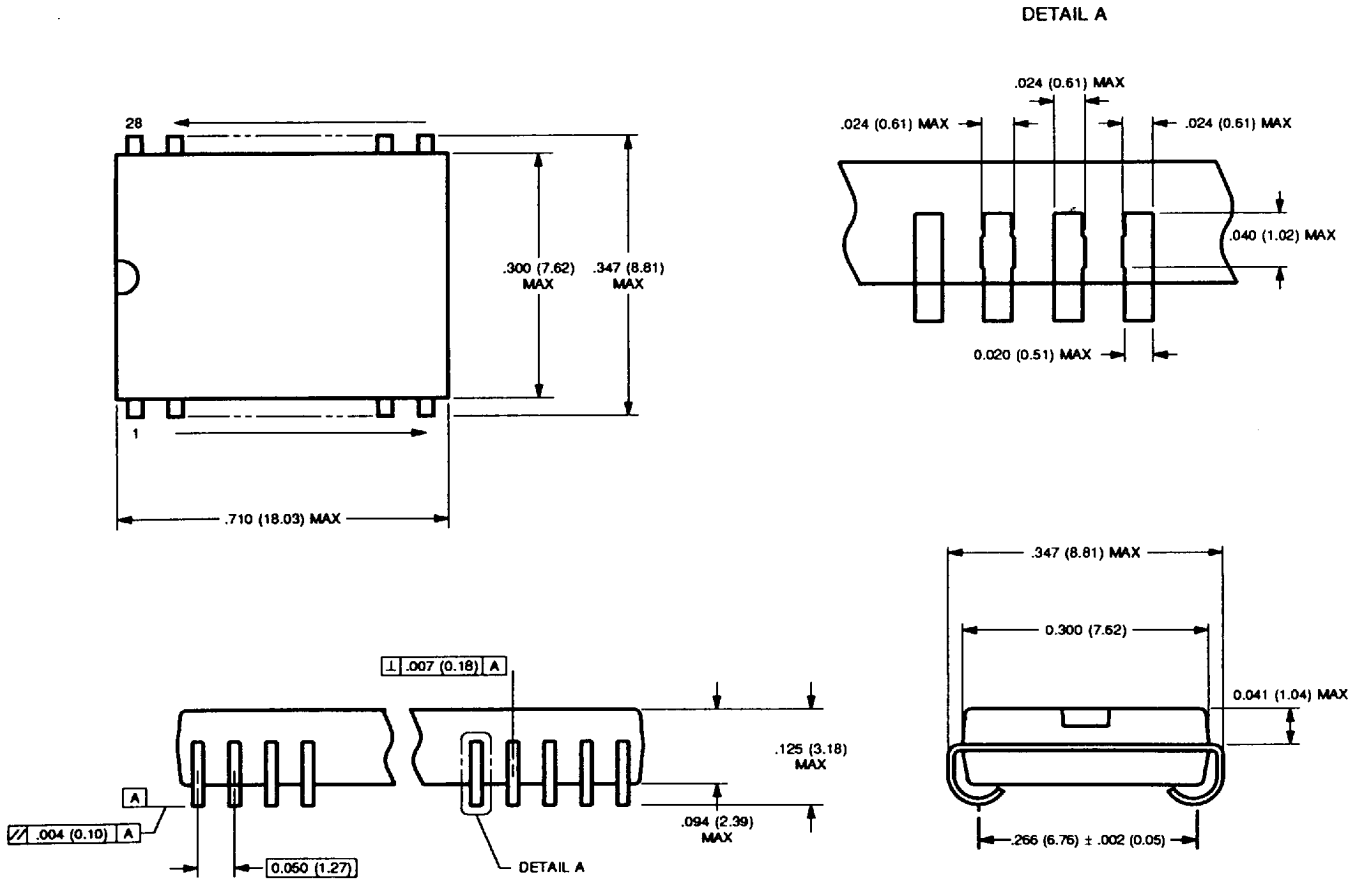
Notes:
Meets JEDEC standards.

Index mark may be a semicircular notch or circular dimple located in the index area.

Outline Diagrams (continued)

28-Pin, Plastic SOJ

Dimensions are in inches and (millimeters).



Note: Index mark may be a notch, dimple, or bevel located in the zone identified on the outline.

Ordering Information

Device Code	Package	Temperature
T7220A-PC	28-Pin, Plastic DIP	0 °C to 70 °C
T7220A-EC	28-Pin, Plastic SOJ	0 °C to 70 °C

Glossary

10BASE-T — A proposed addition to the 802.3 IEEE standard for using twisted-pair wiring as the physical media.

AUI — Attachment unit interface.

CD0 — Clocked data zero. A Manchester-encoding clock signal that is high for the first half of the bit cell and low for the second half of the bit cell.

CD1 — Clocked data one. A Manchester-encoding clock signal that is low for the first half of the bit cell and high for the second half of the bit cell.

CI — AUI collision input circuit.

Collision — A state of collision exists whenever there are valid signals being input to the TPMAU2 from the network and DTE simultaneously and the TPMAU2 is not in a link-failure state.

CS0 Signal — A signal that is placed on the CI circuit whenever a collision condition exists. It is a periodic square wave at 10 MHz ± 15% with a duty cycle no worse than 40/60 or 60/40.

CSMA/CD — Carrier sense multiple access with collision-detect.

DI — AUI data input circuit.

DO — AUI data output circuit.

DTE — Data terminal equipment. Any piece of equipment at which a communication path begins or ends.

HIGH — A logic state of an input.

IDL Pulse — A logic-high pulse of 300 ns ± 50 ns duration that is appended to the end of a data frame to signify the end of the data frame.

Jabber — A function that disables continued transmission of a data frame to the media should that data frame exceed a specified duration.

LAN — Local area network.

Link Integrity — An internal function that determines if a remote MAU is attached and operating at the far end of the twisted-pair link.

LOW — A logic state of an input.

Manchester Encoding — A type of encoding, defined by IEEE 802.3, that ensures transitions are present so that a clock can be recovered from the data stream.

MAU — Medium attachment unit.

ppm — Parts per million.

SQE — Signal quality error.

TP — Twisted pair.

TPMAU2 — Twisted-pair medium attachment unit.