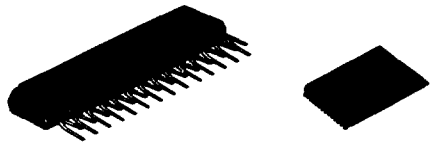
M5M4C500AL,VP-3,-5

491520-BIT(81920-WORD BY 6-BIT)FIELD MEMORY



DESCRIPTION

The M5M4C500A is a field memory consisting of a memory array of 320 rows × 256 columns × 6-bits a serial input memory of 256 × 6-bits, and a serial output memory of 256 × 6-bits. An CMOS process, used with triple-layer polysilicon, has enabled high integration, high speed and low power consumption. A variety of selection operations is possible for data transfer between memory array and serial memory, and specification of row and column address. The selection instructions can be coded by 8 bits and multiplexed to the address pins. The M5M4C500A is housed in a 28-pin ZIP, TSOP package suitable for highly-integrated mounting. This field memory can be used for video signals of NTSC, PAL or SECAM systems.

FEATURES

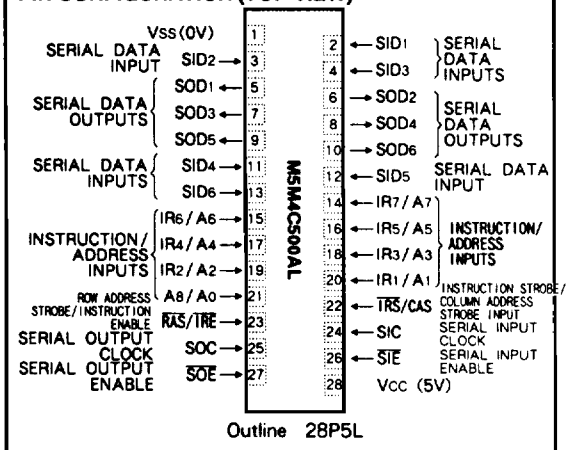
- M5M4C500A Family

Type name	Serial I/O cycle time (min.)(ns)	Serial access time (max.)(ns)	Data transfer cycle time (min.)(ns)	Power consumption (typ)** (mW)
M5M4C500A-3	30	25	390	100
M5M4C500A-5	50	40	810	80

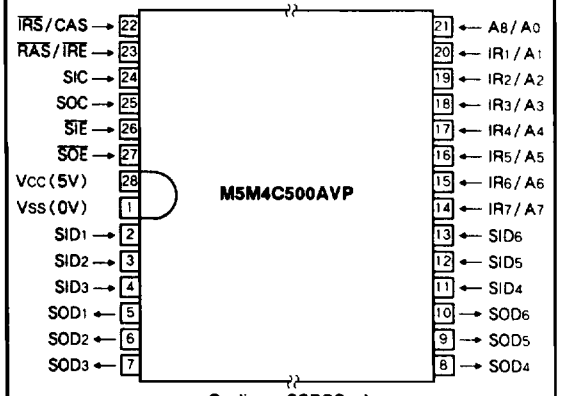
(** ···When Serial input and serial output both operate at the minimum cycle.)

- Memory array configuration most suitable for TV or VCR application·····320 rows × 256 columns × 6-bits
- Large capacity serial memory needs no data transfer during image mode····· 256 × 6-bits (common to input and output sides)
- Serial input and output are operated completely independently or asynchronously.
- Instruction code system avoids complex timing requirements for data transfer or refresh.

PIN CONFIGURATION (TOP VIEW)

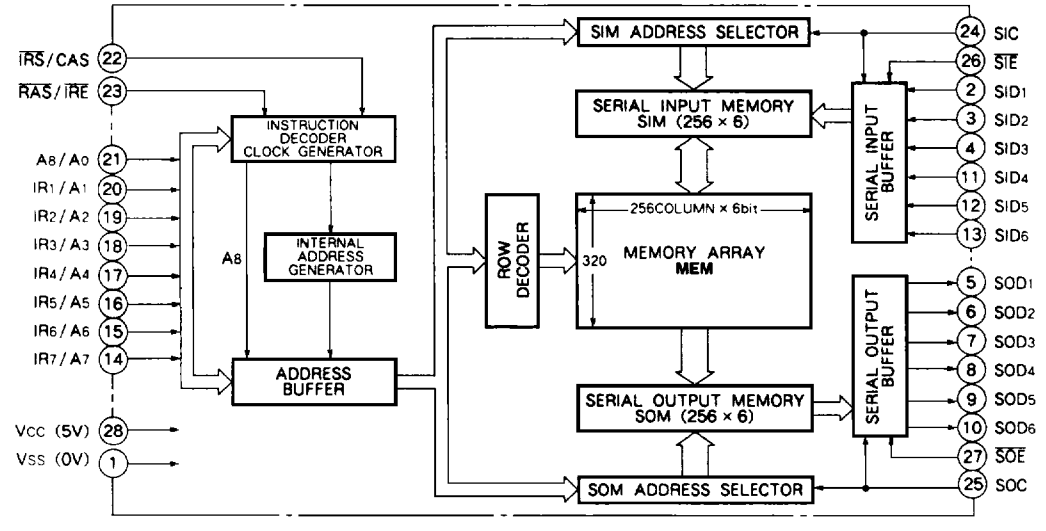


Outline 28P5L



Outline 28P2C-A

BLOCK DIAGRAM



PIN DESCRIPTION

Pin name	Name	I/O	Function
$\overline{IRS}$/CAS	Instruction strobe/column address strobe	Input	This clock reads the 7-bits of instruction code and the most significant bit of the row address at the falling edge and read the 8-bits of column address at the rising edge.
$\overline{RAS}$/$\overline{IRE}$	Row address strobe/instruction enable	Input	This clock reads the 8-bits of row address at the falling edge and ends the execution of instruction at the rising edge. This clock can also be used as instruction execution enable.
A_8/A_0 IR_1/A_1 IR_2/A_2 IR_3/A_3 IR_4/A_4 IR_5/A_5 IR_6/A_6 IR_7/A_7	Instruction code (IR_i) / row address (A_i) / column address (A_i)	Input	The instruction code, row address and column address are multiplexed. Firstly, instruction codes IR_1~IR_7 and the most significant bit of row address A_8 are read in at the falling edge of $\overline{IRS}$/CAS, then secondly, row addresses A_0~A_7 are read in at the falling edge of $\overline{RAS}$/$\overline{IRE}$, and thirdly, column addresses A_0~A_7 are read in at the falling edge of $\overline{IRS}$/CAS.
SIC	Serial input clock	Input	This clock writes serially the 6-bit data at SID_i to the serial input memory (SIM). The data is written at the rising edge of SIC. The SIM address advances to higher bits after the data is written.
$\overline{SIE}$	Serial input enable	Input	Enable writing of the 6-bit data to serial input memory (SIM).
SID_1 ⟆ SID_6	Serial data input (SID_i)	Input	Serial input pin for 6-bit data.
SOC	Serial output clock	Input	This clock reads 6-bit data in the serial output memory (SOM) to SOD_i. The data is accessed at the rising edge of SOC. The output data is stored until the next rising edge of SOC. The address of SOM is advanced after the data is read.
SOE	Serial output enable	Input	Enables reading of 6-bit data of serial output memory (SOM).
SOD_1 ⟆ SOD_6	Serial data output (SOD_i)	Output	Serial output pin for 6-bit data.

- Three-multiplex system of instruction code/row address/column address.
- External row and column addresses can be omitted by internal address functions.
- Long data hold time·····20 msec (320 refresh cycles)
- All inputs, outputs are TTL compatible and low capacitance.
- Single 5V ± 10% power supply.

APPLICATION

Field memory for TV or VCR

1. Summary of operations

1-1 Serial data input

When the serial input enable signal ($\overline{SIE}$) is V_{IL}, the contents of the serial data input ports (SID_1~SID_6) are read in sync with the rising of serial input clock (SIC) and stored in the serial input memory (SIM). The SIM address is set by WTI, RTI and SAI instructions (Refer to 2-2) and is incremented by each SIC input. While the above mentioned instruction is being executed and $\overline{RAS}$/$\overline{IRE}$ = V_{IL}, the SIC input is ignored but the serial output functions can operate independently. Bidirectional data transfers between SIM and memory array are permitted by WTI and RTI instructions.

When $\overline{SIE}$ is V_{IH}, the serial input buffer becomes inactive. Therefore, the contents of SIM is not changed but the SIM address is incremented by each SIC input.

The SIM consists of a dynamic circuit and the minimum data hold time is 1 ms.

1-2 Serial data output

When the serial output enable signal ($\overline{SOE}$) is V_{IL}, the contents of serial output memory (SOM) are transfered to serial data output ports (SOD_1~SOD_6) in sync with the rising edge of the serial output clock SOC. The SOM address is set by RTO and SAO instructions (Refer to 2-2) and is incremented by each SOC input. While the above mentioned instruction is being executed and $\overline{RAS}$/$\overline{IRE}$ = V_{IL}, the SOC input is ignored but the serial input functions can operate independently. Data transfers between SOM and memory array are permitted by RTO instructions.

When $\overline{SOE}$ is V_{IH}, the output ports (SOD_1~SOD_6) are in the high-impedance state and common connections can be made. The SOM address is incremented by each SOC input.

The SOM consistes of static memory.

1-3 Instruction cycle

The instruction cycle is the period in which data transfer, refresh and address setting operations are made. The operations are selected by 8-bits instruction code which avoids complex timing requirement for those operations. The cycle is controlled by two timing signals of $\overline{IRS}$/CAS and $\overline{RAS}$/$\overline{IRE}$, strobing instruction code, row address and column address. Refer to 2-1 for details on the instruction codes.

The basic instruction cycle is shown below.(Fig. 1)

(1) Bring $\overline{IRS}$/CAS low to strobe 8-bits instruction code.
(2) Bring $\overline{RAS}$/$\overline{IRE}$ low to strobe 8-bits row address.
(3) Bring $\overline{IRS}$/CAS high to strobe 8-bits column address.
(4) Bring $\overline{RAS}$/$\overline{IRE}$ high to complete the cycle.

The externally input SIC or SOC is ignored while the $\overline{RAS}$/$\overline{IRE}$ signal is V_{IL}, if the instruction needs address setting of SIM or SOM.

The row or column address input can be omitted for some instructions. If the $\overline{IRS}$/CAS or $\overline{RAS}$/$\overline{IRE}$ signals are not supplied as the specified, the instruction may not be executed or the contents of the memory may be destroyed.

Continuous instruction cycle to execute the instruction continuously for plural number of rows is also possible (See Fig. 3) and is useful for writing the same data to plural rows or for executing burst refresh. In the external row address mode, the most significant bit RA_8 of the row address may not be changed while the continuous instruction cycle is executed because it is given as a part of the instruction code.

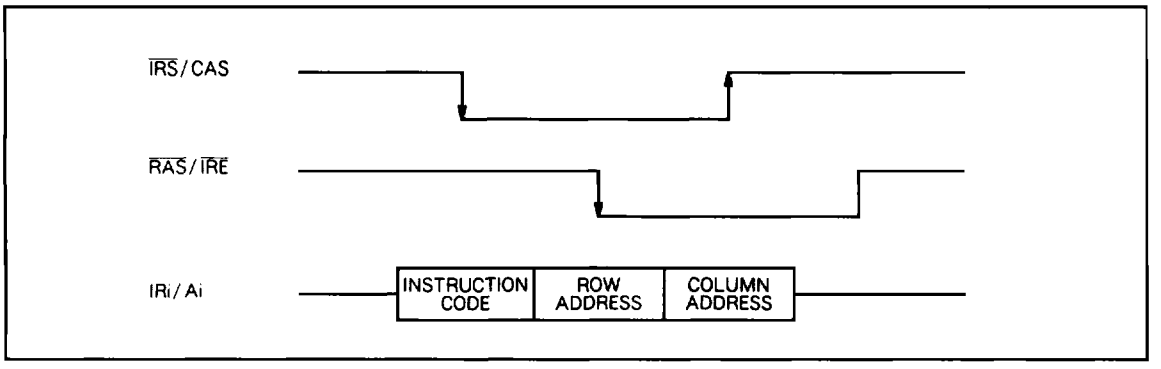


Fig. 1 Basic instruction cycle

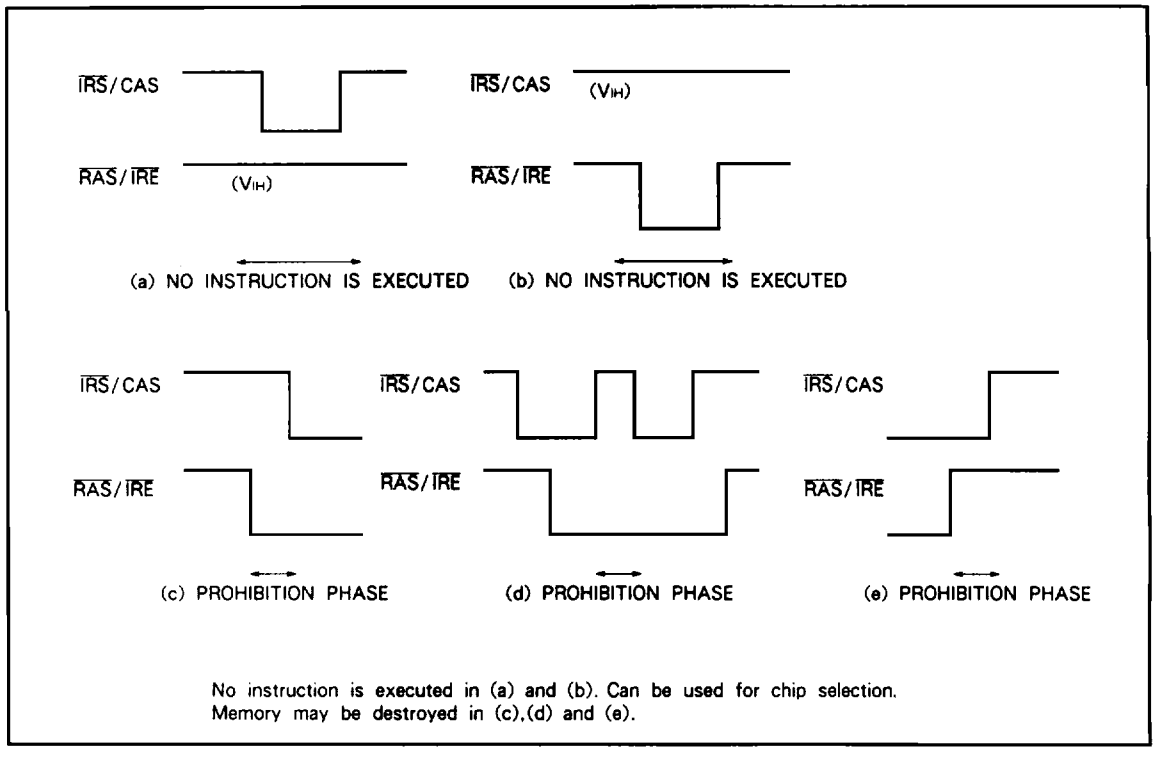


Fig. 2 Precautions for timing signal of instruction cycle

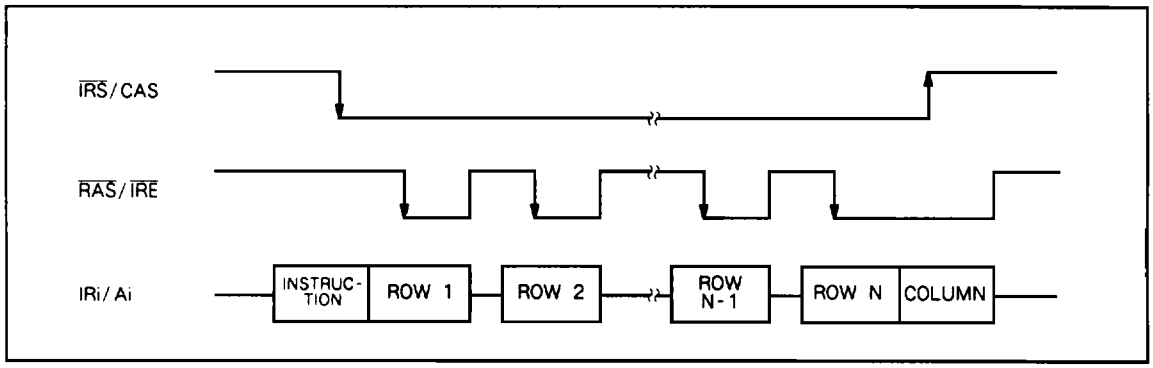


Fig. 3 Continuous instruction cycle

1-4 Refresh and power supply

The memory array consists of a dynamic circuit and the minimum data hold time is 20 ms. If the data needs to be stored for more than 20 ms, refresh is required. The refresh is executed for all instruction cycles (WTI, RTI, RTO, SAI, SAO and REF). If the REF instruction is used, serial input and output are not interrupted. To use the REF instruction cycle, more than 320 REF instruction cycles must be repeated within 20 ms. If all the rows required for data storage are accessed by any data transfer instructions, such as WTI, RTI or RTO, the REF instruction is not needed.

The dynamic circuit is also used for circuits other than memory array and they are refreshed by any instruction cycles of $\overline{IRS}$/CAS and $\overline{RAS}$/$\overline{IRE}$. If the instruction cycle is not executed for more than 20 ms after the power is supplied, eight dummy cycles by $\overline{IRS}$/CAS and $\overline{RAS}$/$\overline{IRE}$ are required. Refer to 1-1 for refresh of SIM.

The substrate bias is given by the internal substrate bias generator. A waiting time of more than 500 μs is required till the substrate bias becomes stable after the power is supplied. The specified memory operation cannot be guaranteed until the substrate bias becomes stable. Special care should be taken so as not to apply rate exceeding voltage to the device during the above-mentioned period.

2. Description of Instruction

2-1 Instruction code

The 8-bit instruction codes are expressed IR_7, IR_6,···IR_1 starting from the most significant bit, and the least significant bit is expressed as A_8. The meaning of each bit of the instruction codes is described as below.

IR_7, IR_6 and , IR_5 specify the row address functions. When $IR_7 = 1$, external row address mode is selected ; when $IR_7 = 0$ and , $IR_6 = 1$, the internal counter mode is selected ; when $IR_7 = 0$ and $IR_6 = 0$, 0 row mode is selected.

IR_5 specifies the incrementation of internal counter value after the instruction is executed. The row address specification is valid when WTI, RTI and RTO instructions are executed.

IR_4 specifies the column address functions. When $IR_4 = 1$, the external column address mode is selected ; when $IR_4 = 0$, 0 Column mode is selected. The column address specification is valid for all instructions except REF instruction.

IR_3, IR_2 and IR_1 specify data transfer and refresh modes. When $IR_3 = 1$, data transfer mode is selected and one of the WTI, RTI and RTO instructions is selected by the combination of IR_2 and IR_1. When $IR_3 = 0$, refresh mode is selected and one of the SAI, SAO, or REF instructions is selected by the combination of IR_2 and IR_1.

A_8 shows the most significant bit RA_8 of the row address in the external row address mode. Detailed description of data transfer / refresh , row address and column address specifications is shown in the following. The instruction code table is shown in Tables 1,2 and 3.

Table 1 Data transfer/refresh specification instruction table

Instruction code / Data transfer/refresh specification instruction	Row address specification code			Column address speccification code	Data transfer/refresh specification code			Row address most significant bit
	IR_7	IR_6	IR_5	IR_4	IR_3	IR_2	IR_1	A_8
WTI Write Transfer from SIM	r_3	r_2	r_1	e	1	1	1	a_8
RTI Read Transfer to SIM	r_3	r_2	r_1	e	1	0	1	a_8
RTO Read Transfer to SOM	r_3	r_2	r_1	e	1	0	0	a_8
SAI Set Address to SIM	X	X	X	e	0	1	1	X
SAO Set Address to SOM	X	X	X	e	0	1	0	X
REF Refresh	X	X	X	X	0	0	X	X

Note 1 : Instruction code symbols are shown below.
0 = V_{IL}
1 = V_{IH}
X = V_{IL} or V_{IH}
r_3, r_2, r_1 is the codes specify row address functions.
e is the code to specify the column address functions.
a_8 is the most significant bit of the external row address.

Table 2 Row address specification instruction table (Note 2)

Row address specification instruction	IR_7 IR_6 IR_5			Row address (Ri) at the instruction	Internal counter value after the instruction
	r_3	r_2	r_1		
External row address mode	1	X	0	(External row address value)	Ri
	1	X	1		Ri + 1
Internal counter mode	0	1	0	(Internal counter value)	Ri
	0	1	1		Ri + 1
0 ROW mode	0	0	0	0	Ri
	0	0	1		Ri + 1

Note 2 : When the internal counter is used, the input row address counter (IRC) is selected for WTI and RTI instructions and the output row address counter (ORC) is selected for RTO instructions automatically.

Table 3 Column address specification instruction table (Note 3)

Column address specification instruction	IR_4	Column address at the instruction
	e	
External column address mode	1	(External column address value)
0 column mode	0	0

Note 3 : The column address of SIM is set for WTI, RTI and SAI instructions : the column address of SOM is set for RTO and SAO instructions.

2-2 Data transfer/refresh specification instruction (See Fig.4)

(i) WTI (Write Transfer from serial Input memory) instruction
This is a write transfer instruction from SIM to memory array. The contents of SIM is transferred to the specified row of memory array, and the next SIM start column address is set.

(ii) RTI (Read Transfer to serial Input memory) instruction
This is a read transfer instruction from memory array to SIM. The contents of the specified row is transferred to SIM, and the next SIM start column address is set. For example, if a part of row data needs to be rewritten, this RTI instruction transfers the row data to SIM, and returns it to memory array again by WTI instruction after the part of data is rewritten.

(iii) RTO (Read Transfer to serial Output memory) instruction
This is a read transfer instruction from memory array to SOM. The contents of the specified row is transferred to SOM, and the next SOM start column address is set.

(iv) SAI (Set Address to serial Input memory) instruction
This is an address setting instruction of SIM. The next SIM start column address is set after the memory array is refreshed. The refresh row address is specified by the internal row address counter (RFC).

(v) SAO (Set Address to serial Output memory) instruction
This is an address setting instruction of SOM. The next SOM start column address is set after the memory array is refreshed. The refresh row address is specified by RFC.

(vi) REF (REFresh) instruction
This instruction refreshes the memory array. The refresh row address is specified by RFC.

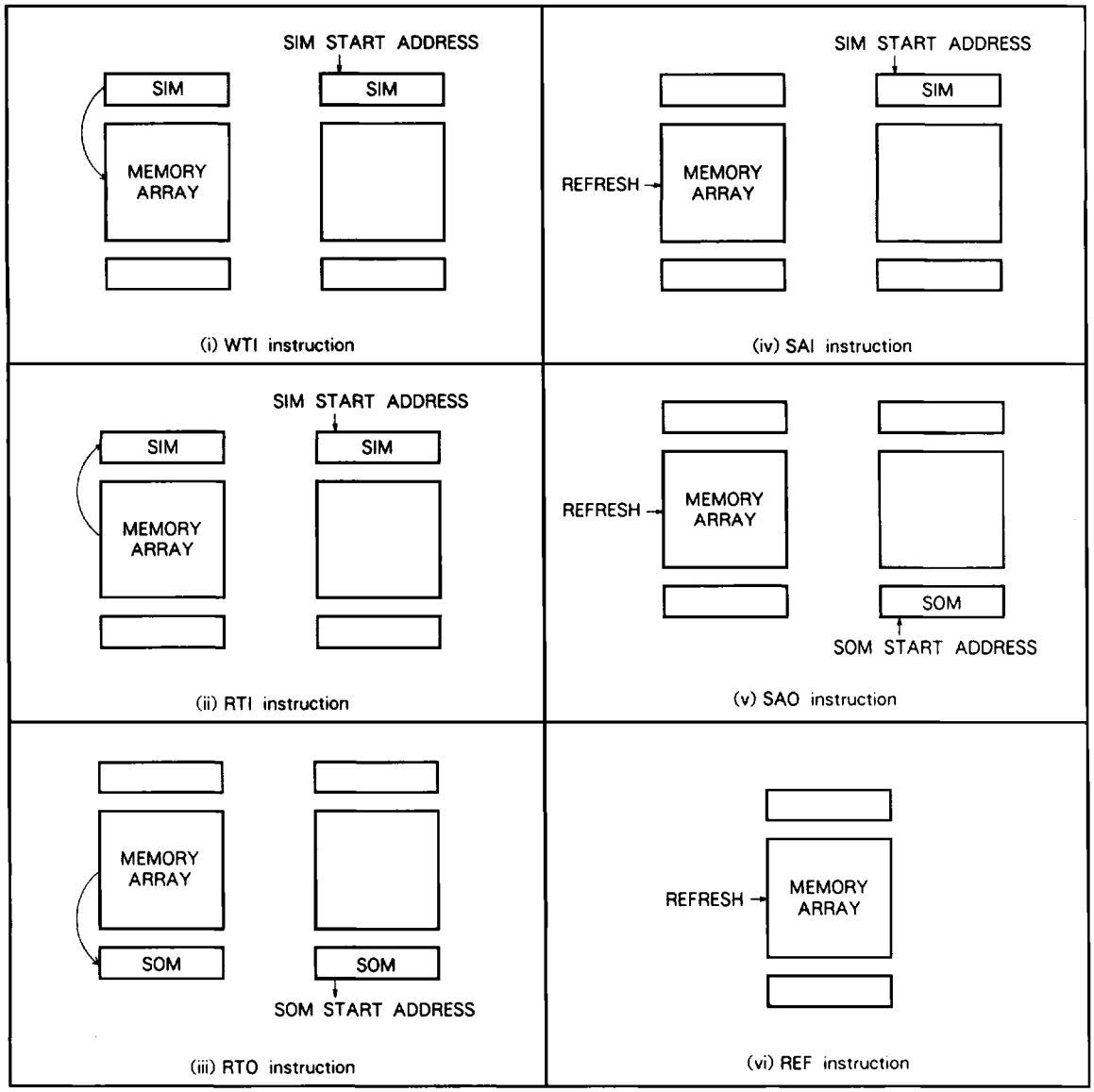


Fig. 4 Operational description of data transfer/refresh instruction

2-3 Row address specification instruction

There are six modes of row address specification when data transfer instructions (WTI, RTI and RTO) are used, including the external row address mode, internal counter mode, 0 ROW mode, and increment specification of internal counter after each mode is executed.

The external row address mode allows reading of row addresses of RA_0 to RA_7 in sync with the falling edge of the $\overline{RAS}/\overline{IRE}$ signal. The most significant bit RA_8 is given as the least significant bit A_8 of the instruction code. Therefore, set $A_8 = 0$ when selecting the address from row 0 to 255, and set $A_8 = 1$ when selecting the address from row 256 to 319. (Do not select addresses for row 320 to 511.)

The internal counter mode allows output from the internal 320-bit row address counter, and external row address input is ignored. When WTI or RTI instruction is used, input-side row address counter (IRC) is automatically selected : when RTO is used, output-side row address counter (ORC) is automatically selected. This makes the row address control easy.

The OROW mode outputs 0 row internally to reset the internal counter. The external row address input is ignored.

If the executed row address is given as R_i, either $R_i + 1$ or R_i is loaded into the internal counter (IRC or ORC) after instruction execution. If $IR_5 = 0$, R_i is loaded : if $IR_5 = 1$, $R_i + 1$ is loaded. The next cycle can take over the internal counter mode. The internal counter mode and OROW mode are sufficient for normal application. Thus, the external row address input can be omitted.

The row address is given from the internal refresh row address counter (RFC) when refresh instructions such as SAI, SAO and REF are used, and row address other than those are not specified.

2-4 Column address specification instruction

SIM start column address is set by WTI, RTI and SAI instructions : SOM start column address is set by RTO, and SAO instructions. The column address specification has external column address mode and 0 Column mode.

The external address mode reads the column addresses CA_0 to CA_7 externally in sync with the rising edge of the $\overline{IRS}/CAS$ signal.

The 0 Column mode outputs the 0 column and the external column address is ignored. In actual application, the start column of SIM or SOM is 0 in most cases, and column address input can be omitted.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	−1~7	V
V_I	Input voltage		−1~7	V
V_O	Output voltage		−1~7	V
I_O	Output current		50	mA
P_d	Maximum power consumption	Ta = 25℃	1000	mW
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		−65~150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = 0~70℃, unless otherwise noted) (Note 4)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		V_{CC}+1	V
V_{IL}	Low-level input voltage, all inputs	−1		0.8	V

Note 4 : All voltage are with respect to Vss.

ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V ± 10%, Vss = 0V, unless otherwise noted) (Note 5)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH} = −1mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL} = 2.1mA	0		0.4	V
I_{OZ}	Off-state output current		Output floating 0V ≤ V_{OUT} ≤ Vcc	−10		10	μA
I_I	Input current		0V ≤ V_{IN} ≤ Vcc, pins not measured are set 0V	−10		10	μA
$I_{CC1\ (AV)}$	Vcc average supply current in instruction cycle (Note 6, 7, 8)	M5M4C500A-3	$\overline{RS}$/CAS, $\overline{RAS}$/$\overline{IRE}$ cycling SIC = SOC = V_{IL}, t_{RC} = minimum, outputs are open		10	20	mA
		M5M4C500A-5			10	20	
I_{CC2}	Vcc average supply current during stand-by		$\overline{RS}$/CAS = $\overline{RAS}$/$\overline{IRE}$ = V_{IH}, SIC = SOC = V_{IL}, outputs are open		2	4	mA
$I_{CC3\ (AV)}$	Vcc average supply current during serial input (Note 6, 8)	M5M4C500A-3	$\overline{RS}$/CAS = $\overline{RAS}$/$\overline{IRE}$ = V_{IH}, SIC cycling, SOC = V_{IL}, t_{SCC} = minimum, outputs are open		10	20	mA
		M5M4C500A-5			8	15	
$I_{CC4\ (AV)}$	Vcc average supply current during serial output (Note 6, 7, 8)	M5M4C500A-3	$\overline{RS}$/CAS = $\overline{RAS}$/$\overline{IRE}$ = V_{IH}, SIC = V_{IL}, SOC cycling, t_{SCC} = minimum, outputs are open		10	20	mA
		M5M4C500A-5			8	15	
$I_{CC5\ (AV)}$	Vcc average supply current at worst combination (Note 6, 7, 8)	M5M4C500A-3	$\overline{RS}$/CAS, $\overline{RAS}$/$\overline{IRE}$ cycling, SIC, SOC cycling t_{RC}, t_{SCC} = minimum, outputs are open		30	60	mA
		M5M4C500A-5			26	50	

Note 5. Current flowing into the IC is positive (no sign).
6. $I_{CC1\ (AV)}$, $I_{CC3\ (AV)}$, $I_{CC4\ (AV)}$ and $I_{CC5\ (AV)}$ are dependent on cycle time. The specified value is measured at the minimum cycle time.
7. $I_{CC1\ (AV)}$, $I_{CC4\ (AV)}$ and $I_{CC5\ (AV)}$ are dependent on output load. The specified value is measured when outputs are open.
8. If plural number of operating modes are executed, the supply current is the sum of each supply current. The supply current becomes most by the combination of instruction cycle, serial input and output. I_{CC5} = I_{CC1} + I_{CC3} + I_{CC4}.

I/O CAPACITANCE (Ta = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C_{I1}	Input capacitance, address inputs	V_{IN} = Vss f = 1MHz Vi = 25mVrms (V_{OUT} = Vss)		3	5	pF
C_{I2}	Input capacitance, data inputs			4	6	pF
C_{I3}	Input capacitance, clock inputs			5	7	pF
C_O	Output capacitance, data outputs			5	10	pF

TIMING REQUIREMENT (Ta = 0~70℃, Vcc = 5V ± 10%, Vss = 0V, unless otherwise noted) (Note 9, 10)

Symbol		Parameter	Limits M5M4C500A -3 Min	-3 Max	-5 Min	-5 Max	Unit
t_{IR}	#1	$\overline{IRS}$/CAS low pulse width	240		400		ns
t_{IRP}	#2	$\overline{IRS}$/CAS high pulse width	150		400		ns
t_{IRD}	#3	Delay time, $\overline{IRS}$ low to $\overline{RAS}$ low	90		150		ns
t_{RCD}	#4	Delay time, $\overline{RAS}$ low to $\overline{IRS}$ high	150		250		ns
t_{CAS}	#5	Delay time, $\overline{IRS}$ high to $\overline{RAS}$ high	90		150		ns
t_{RAS}	#6	$\overline{RAS}$/$\overline{IRE}$ low pulse width	240	2000	400	2000	ns
t_{RP}	#7	$\overline{RAS}$/$\overline{IRE}$ high pulse width	150		400		ns
t_{RC}	#8	Row address cycle time	390		810		ns
t_{IRS}	#9	Instruction code setup time before $\overline{IRS}$ low	0		0		ns
t_{IRH}	#10	Instruction code hold time after $\overline{IRS}$ low	30		50		ns
t_{ASR}	#11	Row address setup time before $\overline{RAS}$ low	0		0		ns
t_{AHR}	#12	Row address hold time after $\overline{RAS}$ low	30		50		ns
t_{ASC}	#13	Column address setup time before high	0		0		ns
t_{AHC}	#14	Column address hold time after $\overline{IRS}$ high	30		50		ns
t_{SRS}	#15	Serial-clock high setup time before $\overline{RAS}$ low	30		100		ns
t_{SRH}	#16	Serial-clock low hold time after high	20		20		ns
t_{SCH}	#17	Serial-clock high pulse width	10		20		ns
t_{SCL}	#18	Serial-clock low pulse width	10		20		ns
t_{SCC}	#19	Serial-clock cycle time	30		50		ns
$t_{h\ (SEH)}$	#20	$\overline{SIE}$ high-level hold time after SIC high	10		20		ns
$t_{su\ (SEL)}$	#21	$\overline{SIE}$ low setup time before SIC high	10		20		ns
$t_{h\ (SEL)}$	#22	$\overline{SIE}$ low hold time after SIC high	10		20		ns
$t_{su\ (SEH)}$	#23	$\overline{SIE}$ high setup time before SIC high	10		20		ns
t_{DS}	#24	Serial input data setup time before SIC high	0		0		ns
t_{DH}	#25	Serial input data hold time after SIC high	20		20		ns
t_T	#26	Transition time (rising and falling time)	0	50	0	50	ns
t_{REF}	#27	Memory cell data hold time		20		20	ms

Note 9 : An initial pause of 500 μs is required after power-up followed by any eight $\overline{IRS}$/CAS and $\overline{RAS}$/$\overline{IRE}$ cycles before proper device operation is achieved.
Note that $\overline{IRS}$/CAS or $\overline{RAS}$/$\overline{IRE}$ may cycled during the initial pause.
And any 8 $\overline{IRS}$/CAS and $\overline{RAS}$/$\overline{IRE}$ cycles are required after prolonged period of $\overline{RAS}$/$\overline{IRE}$ inactivity before proper device operation is achieved.

10 : Timing requirements are assumed t_T = 5ns. Timing specification level of the input signal is V_{IH} (min) and V_{IL} (max).

11 : t_T is the transition time between V_{IH} (min) and V_{IL} (max).

* The SIM consists of a dynamic circuit and the minimum data hold time is 1ms.

SWITCHING CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V ± 10%, Vss = 0V, unless otherwise noted)

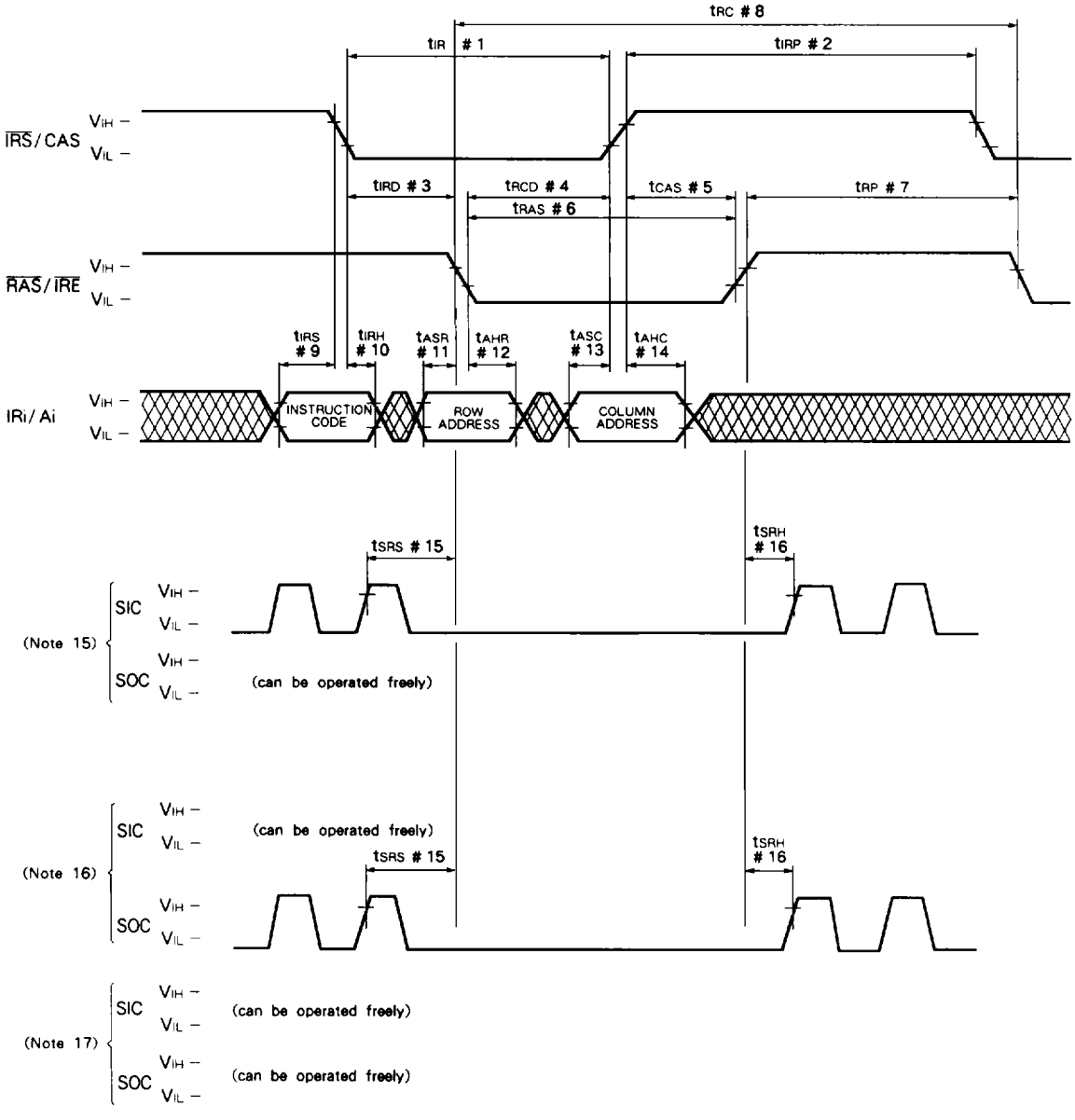
Symbol		Parameter		Limits M5M4C500A -3 Min	-3 Max	-5 Min	-5 Max	Unit
t_{SCA}	#28	SOC access time	(Note 12)		25		40	ns
t_{SOH}	#29	Output data hold time after SOC	(Note 12)	5	20	10	30	ns
t_{SEA}	#30	Output enable time after $\overline{SOE}$ low	(Note 12)		30		30	ns
t_{SEZ}	#31	Output disable time after $\overline{SOE}$ high	(Note 13)		20		20	ns

Note 12 : Measured with a load circuit equivalent to 1TTL load and 100pF. The timing specification level of the output signal is V_{OH} (min) and V_{OL} (max).

13 : t_{SEZ} is defined when the output circuit enters the high-impedance state and not when it becomes V_{OH} or V_{OL}.

TIMING DIAGRAM (Note 14)

Instruction cycle



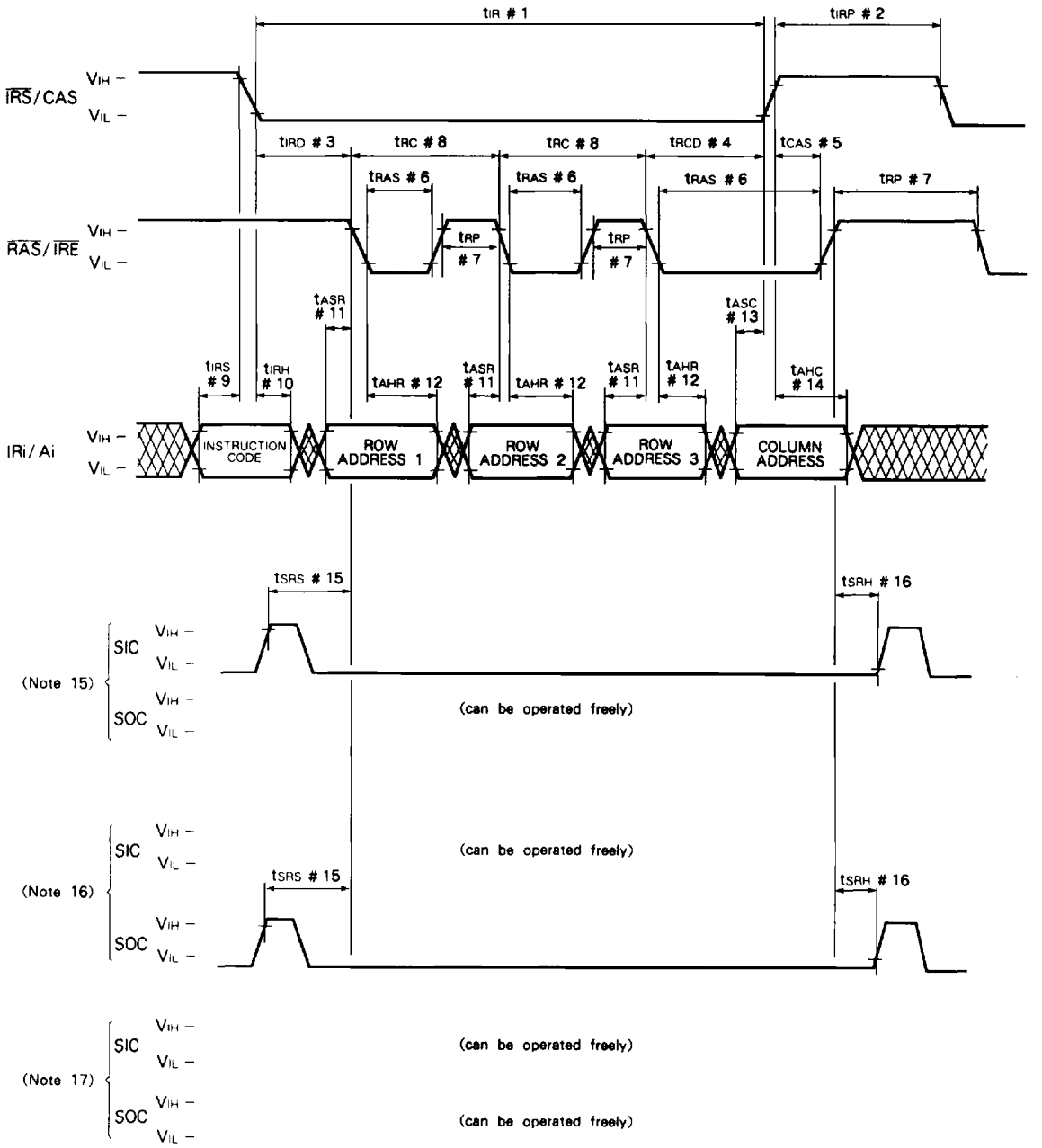
Note 14 : Indicates the don't care inputs.

15 : Indicates operation when WTI, RTI and SAI instructions are used.

16 : Indicates operation when RTO and SAO instructions are used.

17 : Indicates operation when REF instructions is used.

Continuous instruction cycle



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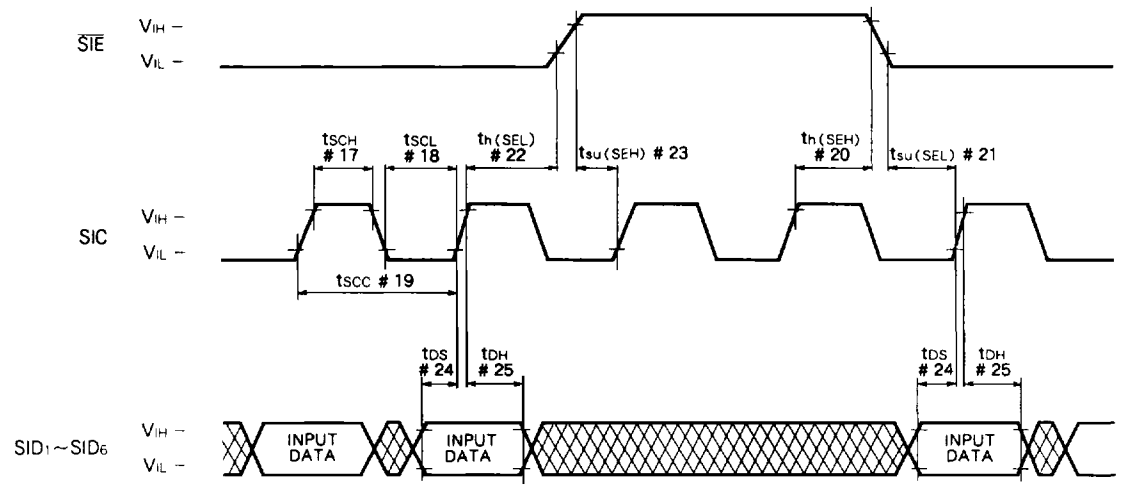
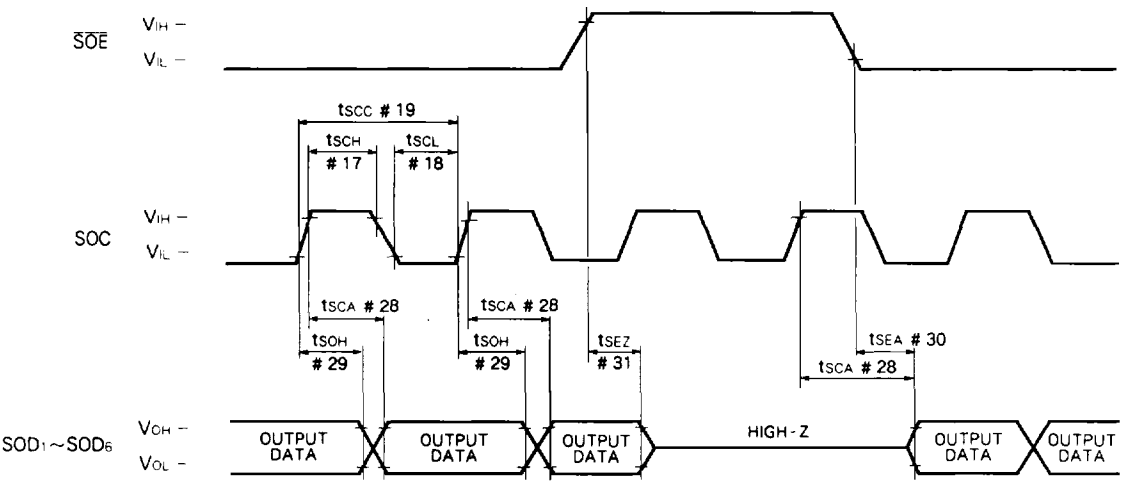
Serial input cycle



Serial output cycle



5. Application example

5-1 Moving picture and still picture (Fig. 5)

Moving picture mode allows data input to update the screen as well as the data output from the memory to screen. If the data input is stopped, the screen will display a still picture. The memory reads the input data in sync with the SIC signal to SIM and transfers to memory array by WTI instruction. The data in the memory array is transferred to SOM in sync with the SOC signal by RTO instruction. If due care is taken that the WTI and RTO instructions are not selected at the same time, no complex synchronous control of input and output is required and the system can be easily designed.

Examples of instruction codes for the moving/still picture mode are shown below. Note the row address is up to 255 rows and the column start address is 0. WTI instruction is excluded when the still picture is displayed.

5-2 Reduced picture(Fig. 6)

The reduced picture function displays a field of data in reduced size for split-screen or picture-in-picture modes.

In this memory operation, input data are sampled at a longer interval than that of moving/still pictures, and a reduced screen is obtained in the memory. The output operates in the same manner as in the moving/still picture. Care should be taken that the contents of columns other than those used for the reduced picture are destroyed by WTI instruction. If the previous data needs to be un-changed, the data in the memory array should be transferred to SIM by RTI instruction and the data of the reduced picture should be sampled.

Examples of instructions used for reduced picture are shown below. Note the row address is up to 255 rows and the column start address of reduced picture is Cj. The RTO instruction operates in the same way as in the moving/still picture mode.

Table 4 Instruction code examples for the moving/still picture

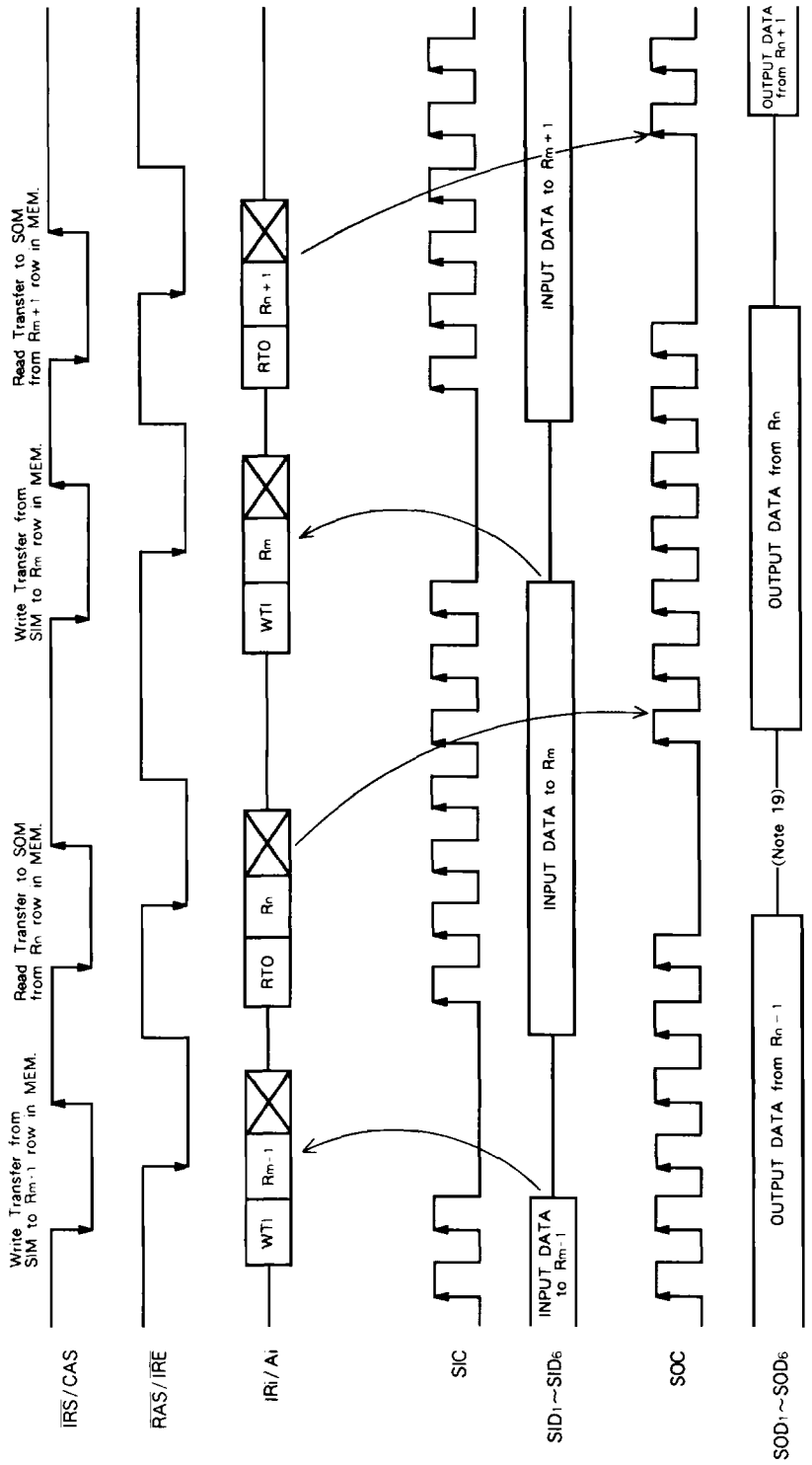
	Instruction	Instruction code input IR_7 ..... IR_1, A_8								Row address input	Column address input
External row address mode	WTI	1	1	1	0	1	1	1	0	Rm	X
	RTO	1	1	1	0	1	0	0	0	Rn	X
Internal row address mode (Note 18)	WTI	0	r	1	0	1	1	1	0	X	X
	RTO	0	r	1	0	1	0	0	0	X	X

Note 18 : When the row address is 0, r = 0. When the row address is not 0, r = 1.

Table 5

	Instruction	Instruction code input IR_7 ..... IR_1, A_8								Row address input	Column address input
External row address mode	RTI	1	1	0	1	1	0	1	0	Rm	Cj
	WTI	1	1	1	1	1	1	1	0	Rm	X (Note 20)
Internal row address mode (Note 18)	RTI	0	r	0	1	1	0	1	0	X	Cj
	WTI	0	1	1	1	1	1	1	0	X	X

Note 20 : The column address is set by RTI instruction after WTI instruction is executed.



$\overline{SIE}$ and $\overline{SOE}$ are V_{IL}.

Note 19: During this period, the last accessed output data is maintained. If $\overline{SOE}$ is V_{IH} the output becomes Hi-Z.

Fig. 5 Memory operation of moving/still picture

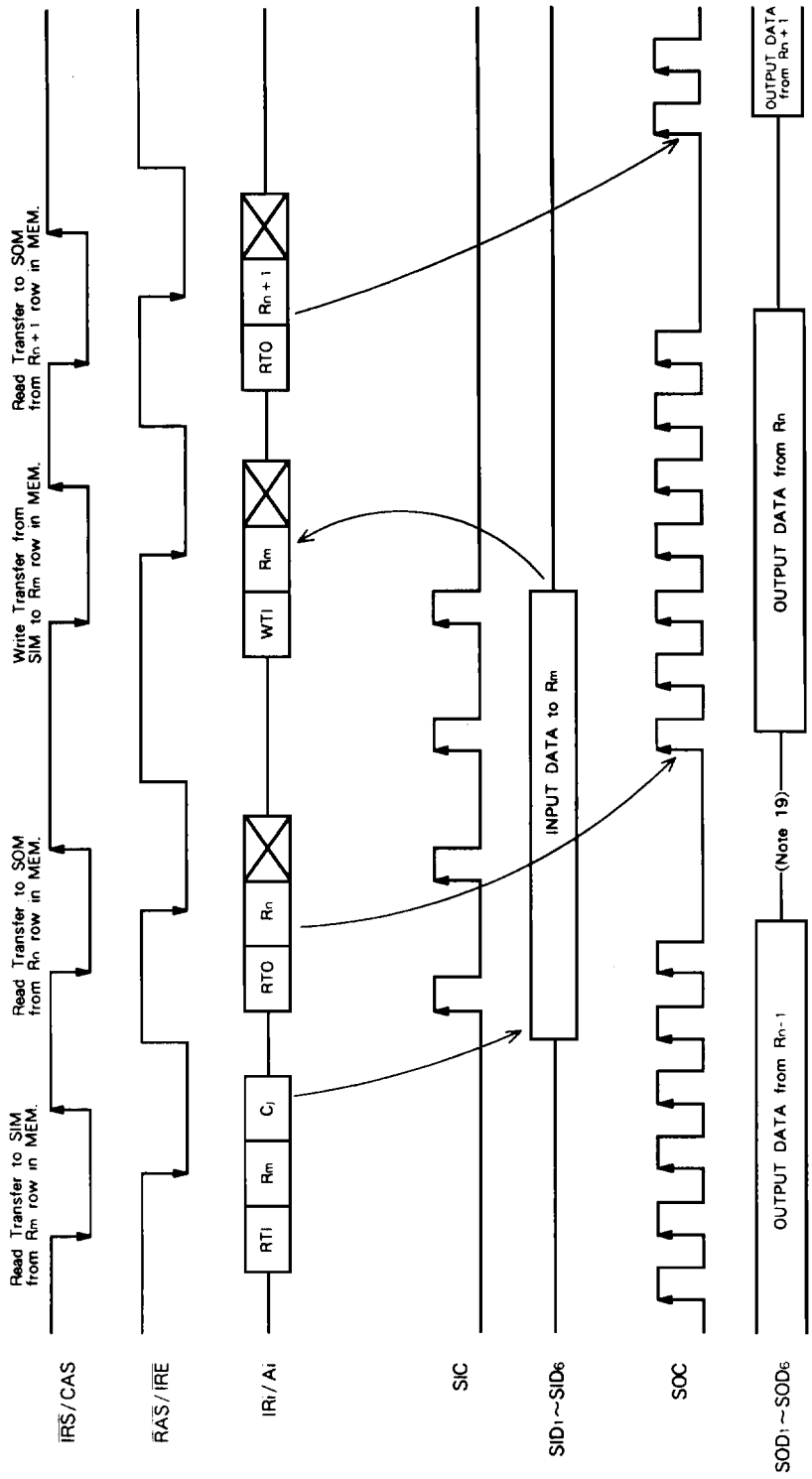


Fig. 6 Memory operation for reduced picture

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5-3 Common connection of serial input and output (Fig. 7)

To make common connection of plural elements of serial inputs $SID_1 \sim SID_6$, SIC signal should be given to each element and the input timing of data should be controlled by giving different SIC signals to each element. (Fig. 8-a)

If the serial outputs $SOD_1 \sim SOD_6$ are connected commonly, SOC and $\overline{SOE}$ signals should be given differently for each element and care should be taken to prevent confliction of output data. That is, avoid V_{IL} overlapping for $\overline{SOE}$ inputs of the elements. The SOC and $\overline{SOE}$ signals can be shared in the following structure as shown in Fig. 8-b.

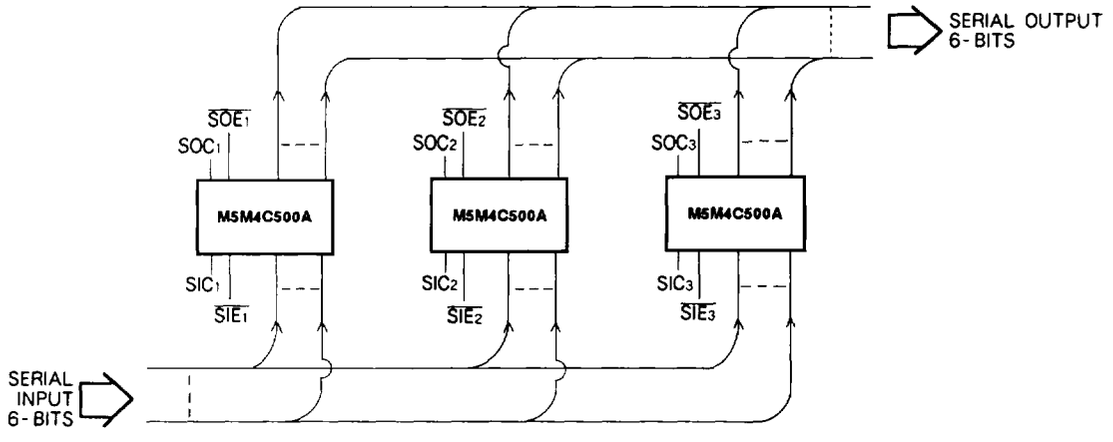
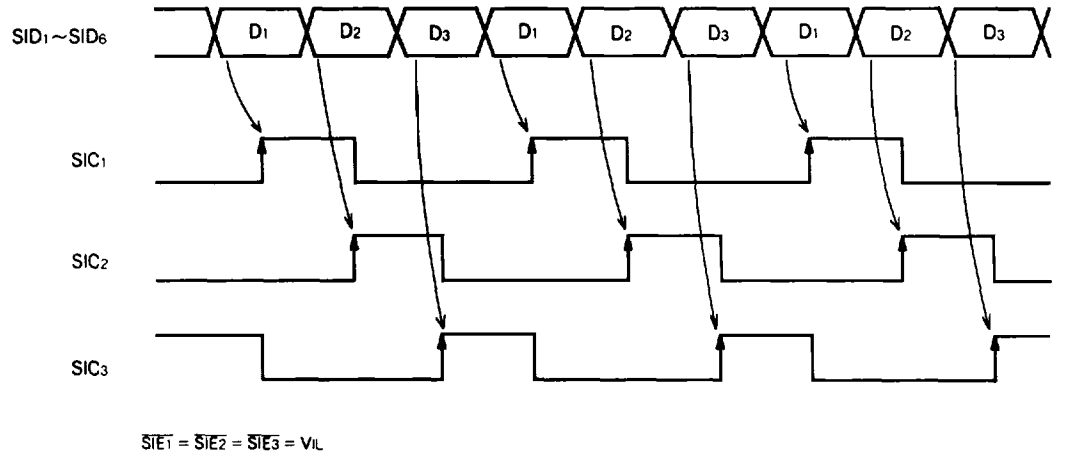
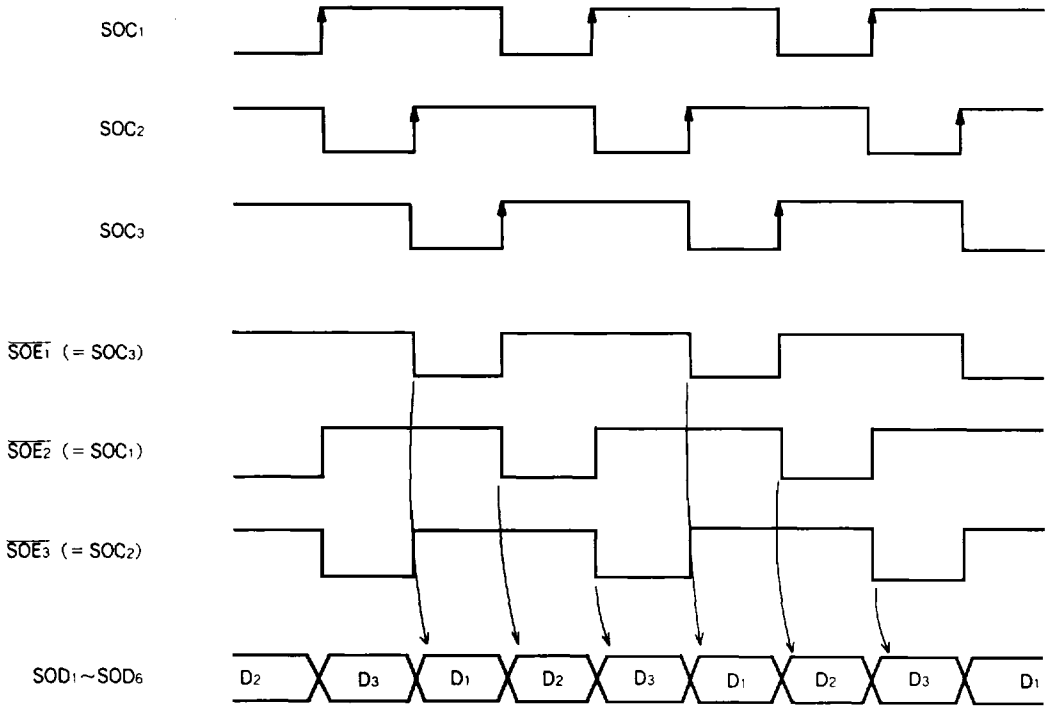


Fig. 7 Common connection of serial I/O



$\overline{SIE1} = \overline{SIE2} = \overline{SIE3} = V_{IL}$

(a)



(b)

Fig. 8 Example of signals for common connection of serial I/O

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6. The using difference point of M5M4C500A and M5M4C500L

(1) The elimination of WTO forward function (See Table 5)
(2) The change of serial memory data hold time (See Fig. 9)

Table 6

	Data transfer/refresh specification instruction	M5M4C500A	M5M4C500L
WTI	Write Transfer from SIM	○	○
WTO	Write Transfer from SOM	×	○
RTI	Read Transfer to SIM	○	○
RTO	Read Transfer to SOM	○	○
SAI	Set Address to SIM	○	○
SAO	Set Address to SOM	○	○
REF	Refresh	○	○

○ : PERMISSION × : PROHIBITION

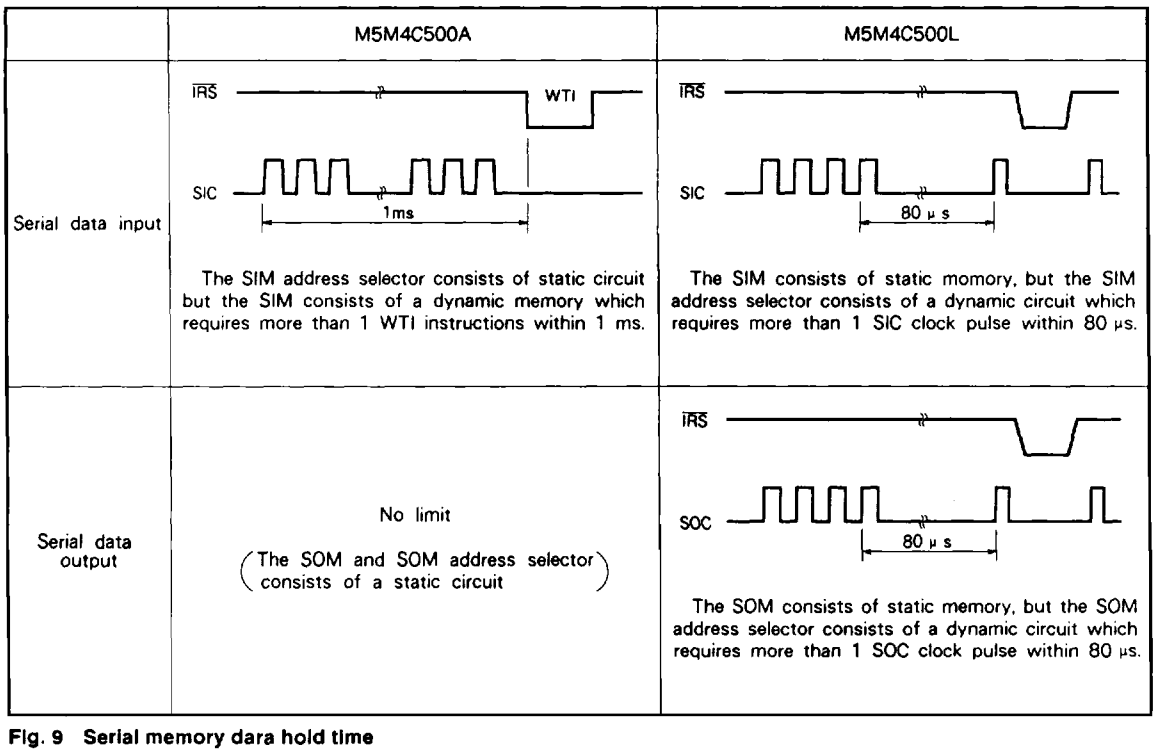

Fig. 9 Serial memory dara hold time