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Application Note

USER CONSIDERATIONS FOR MC146818 REAL TIME CLOCK APPLICATIONS

Prepared by
Patrick Svatek
System Applications Engineering Department
Motorola, Inc.
Austin, Texas

INTRODUCTION

This application note provides information concerning the use of a 32 kHz oscillator and battery backup with the MC146818 real time clock (RTC). Although three different oscillator frequency inputs can be used with the RTC, the 32 kHz oscillator was selected for this application note because it consumes the least power. Two circuits for integrating battery backup into a design are also presented.

In review, the MC146818 RTC plus RAM is a CMOS peripheral device which includes; a complete time-of-day clock with alarm and a 100-year calendar, a periodic interrupt and square-wave generator. The MC146818 utilizes high speed CMOS technology which allows it to interface with processor buses while consuming very little power. The low power consumption feature makes this device ideal for use in a battery backup environment. For a complete list of features available on the RTC, consult the MC146818 data sheet.

TIME-BASE TRADE-OFF

The MC146818 RTC is capable of operating with three different time base input options: 4.194304 MHz, 1.048576 MHz, and 32.768 kHz. Selection of the appropriate time base usually consists of an accuracy versus power consumption trade off. The 32 kHz time base minimizes power consumption since fewer active transitions per unit-of-time occur and less divider stages are required. The 4.194304 MHz mode provides the maximum time keeping accuracy, while the 1.048576 MHz operation is a good compromise between accuracy and power consumption. Connections for the 4 MHz and 1 MHz operation are shown in the MC146818 data sheet.

32 kHz OSCILLATOR

A schematic diagram of the external components required for a typical 32.768 kHz square-wave oscillator circuit is shown in Figure 1. This uses a single on-chip inverter, two resistors, two capacitors, and a tuning fork quartz-type crystal configured as a Pierce oscillator. The crystal behaves electrically as an inductor, thus, the two capacitors and the crystal provide the necessary 180-degree phase shift in the feedback loop. The actual operational frequency is 30 to 300 parts per million (ppm) above the series resonant frequency of the crystal.

Resistor R1 is a bias resistor with its value chosen to ensure linear region operation of the inverter. The value of R1 should be large enough (22 megohms typical) so as not to affect the phase shift of the feedback network, yet low enough to guarantee linear operation. Decreasing the value of R1 lowers loop gain and increases bandwidth. Overdrive protection for the crystal is provided by the voltage divider formed between resistor R2 and capacitor C2. This network also swamps amplifier output impedance variations. Capacitor C2 introduces phase shift in the feedback circuit. Large C2 values stabilize the oscillator during power supply variations; however, large C2 values also reduce the tuneability of the circuit. Variable capacitor C1 allows for a limited adjustment of the output frequency. Capacitors C1 and C2 form the load capacitance for the crystal. The load capacitance is given by:

$$C_L = \frac{C1 + C2}{C1 \times C2} + C_S$$

where C_S is the stray capacitance.

The 32 kHz crystal used in this oscillator circuit is physically small, of unusual technology, and is not readily available from all crystal manufacturers. The two manufacturers that furnished crystals for this application note are listed in Table 1. The crystal for each manufacturer functioned satisfactorily. Different values of C1 and C2 are required with each manufacturer's crystal. Additionally, the input drive level requirements vary. The Pierce oscillator is

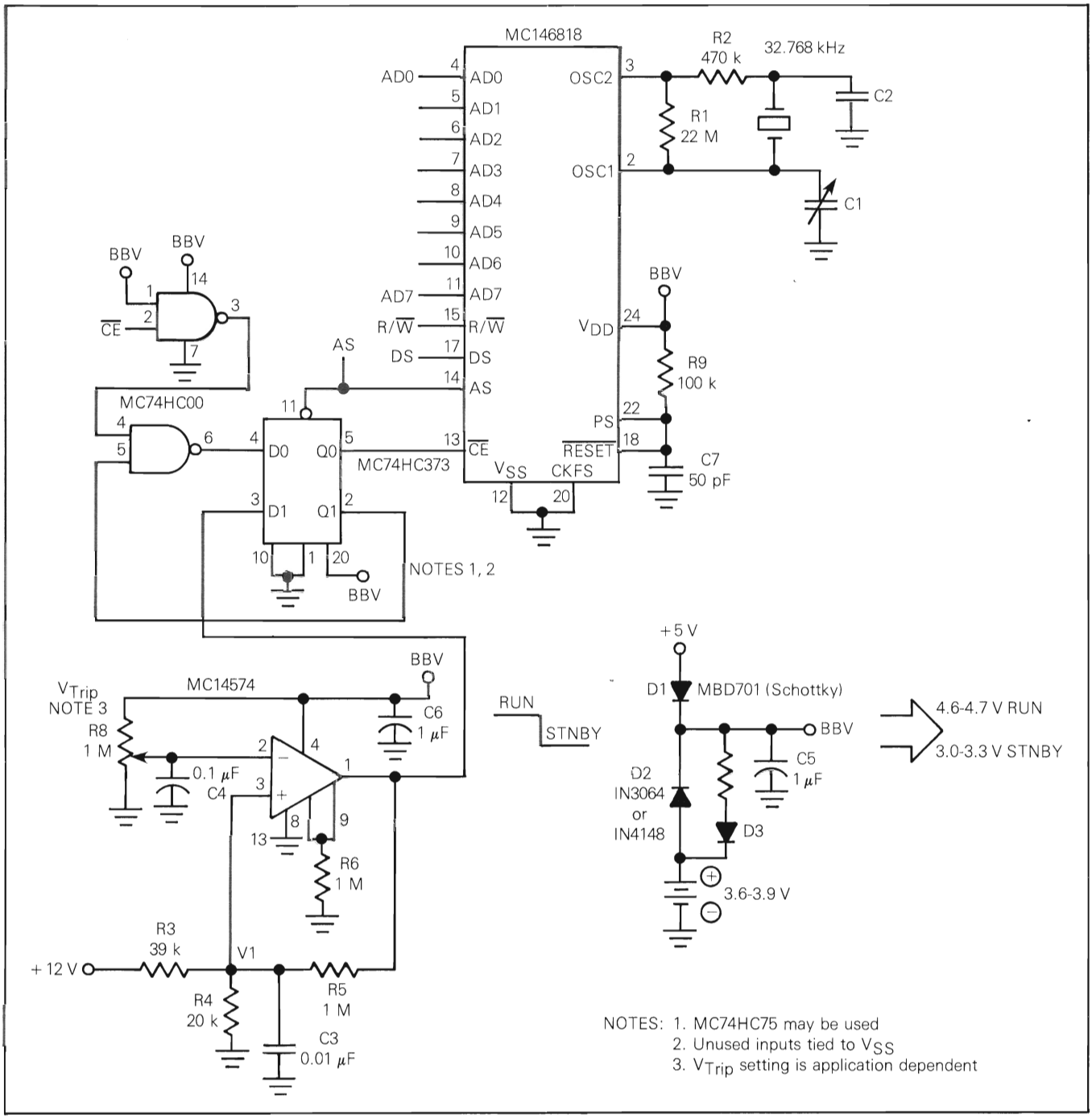

FIGURE 1 — MC146818 Interfacing-Schematic Diagram

slower starting than a series resonant circuit. Start up times varied, but were typically less than one second.

ADDITIONAL CONSIDERATIONS

The 32 kHz oscillator used for this application note functions properly and exhibits relatively good frequency stability over ambient temperature ranges; however, there is a possibility of minor frequency variations resulting from voltage fluctuation. Using the circuit component values shown in Figure 1, the oscillator reacts only slightly to a decrease in V_{DD} from 5 volts down to 3.9 volts. The actual change in frequency over this 1.1-volt range would be about 0.1 Hz and could result in an error of about 7.9 seconds per month. The value of resistor R2 value is important in maintaining frequency stability. With R2 selected as 330k ohms, the oscillator is very sensitive to the values of capacitors C1 and C2 and at times the R2 value must be chosen to match the crystal. With R2 decreased in value to 2k ohms, the oscillator is less sensitive to C1 and C2; however, it is considerably more prone to frequency changes resulting from voltage variations. In normal operation, an increase in supply voltage should increase the operating frequency (a few ppm). If the crystal is being overdriven due to a low value of R2, an increase in voltage causes a decrease in frequency or an unstable frequency. For example, with R2 at a value of 2k ohms, a 1.1 volt change in V_{DD} could result in a

TABLE 1 — Crystal Parameters/Manufacturer

Crystal Manufacturer	C1	C2
STATEK	0-20 pF	5-40 pF
SEIKO	7-25 pF	27 pF
STATEK Corporation 512 N. Main St. Orange, Ca. 92668 Phone 714-639-7810	SEIKO Instruments U.S.A., Inc. 2990 W. Lomita Blvd. Torrance, Ca. 90504 Phone 213-530-8777	

1.2 Hz frequency change. This amounts to an error of 87 seconds in a month. The CKOUT pin (21) of the RTC provides a buffered oscillator output to observe oscillator frequency directly if the CKFS pin (20) is tied to V_{DD}.

For cases where errors of 7.9 or 87 seconds are not acceptable, two options are suggested. The first, and possibly the easiest to implement, is to keep the battery backup voltage equal to V_{DD}. This requires a slightly higher power consumption from the backup battery but the frequency drift is lessened or eliminated. A second method is to use a voltage and temperature compensated oscillator to provide a stable 32.768 kHz source. The latter method is more complex and requires more power; however, in systems where accurate time is a requirement, a simple oscillator is not adequate. Higher frequency crystals exhibit similar voltage-frequency drift characteristics even when attached directly to the MC146818.

The total current (I_{DD}) at 32 kHz operation may be higher than expected if good printed circuit board (PCB) layout rules are not followed. Low voltage oscillator circuits exhibit high impedances making them susceptable to noise, especially from address/data lines. Switching signals should be isolated from the oscillator circuit by using ground planes. Standard wire-wrapping techniques are not acceptable for building prototypes where I_{DD} must be measured accurately. These circuits should be built on perforated board to minimize stray capacitances wherever possible. By inserting a 100 ohm resistor in series with the V_{DD} power line, then measuring across the resistor, the total operating current may be measured. With good layout techniques, 3-volt operation should consume about 50-75 microamperes. Note that the total current in the circuit is made up of the normal IC leakage currents plus the oscillator current, and that its magnitude is PCB layout dependent.

BATTERY BACKUP AND INTERFACING

A battery backup for the MC146818 is extremely useful in many applications. Since there is no specific pin on the RTC for sensing a power shutdown condition, the $\overline{CE}$ pin must be used to perform a dual function. The first use of this pin is the normal chip select function associated with memory-mapped peripherals. The second use of the $\overline{CE}$ line is to isolate the RTC from a system that is being powered down, thus providing memory retention by avoiding spurious writes to RAM or other registers. When the $\overline{CE}$ pin is not used, it should be grounded.

BATTERY BACKUP CIRCUIT

In order to provide a smooth transition from main power to battery backup operation, a power sensing circuit with early detection must be devised. Simple detection circuits, such as a single Schmitt trigger, are not acceptable because during the time between power loss and trigger output, the MPU may have become unstable. For example, an MPU with a V_{DD} minimum of 4.75 volts is not guaranteed to operate properly below that value, and the threshold of a Schmitt trigger operated at 5.0 volts is not 4.75 volts.

Because of the random nature of power failures, a recognition point in the bus cycle timing should be chosen to ensure that no partial accesses can occur. This function is easily implemented by using a transparent latch (MC74HC373 or MC74HC75) that only selects or deselects the chip enable ($\overline{CE}$) on the RTC, while the time address strobe (AS) is high. Hence, a change in the state of $\overline{CE}$ due to a normal chip select or a power failure is honored once each bus cycle.

One efficient method of sensing a power shutdown condition is to use a battery powered comparator circuit, as shown in Figure 1. The comparator controls the $\overline{CE}$ pin of the RTC. One input at comparator pin 2, obtained from battery voltage BBV via potentiometer R8, provides the +3-volt reference level. Voltage divider R3, R4 is connected to an unregulated +12 volts. In turn, the R3, R4 junction (node V1) provides the +4-volt (normal operation) power-sense input at comparator pin 3. When the voltage at node V1 falls below the +3-volt reference level at the other comparator input, the comparator toggles and deselects the MC146818 ($\overline{CE}$ goes high) after two address strobe pulses have occurred. The comparator configuration also uses a small amount of hysteresis for improved noise immunity. The +3-volt setting on potentiometer R8 equates to a comparator trip when the main supply falls to +9 volts. At this level, sufficient V_{DD} margin is maintained to ensure that the required two address strobes occur, before the MPU bus becomes unstable. The trip point on the comparator may be changed to suit individual systems. If only +5 volts is available for voltage sensing, the trip point should be set close enough to the reference point to allow for the required two address strobes to arrive at the MC74HC373 after the comparator trips, but still allow for system V_{DD} margin. In a +5-volt system the reference and sense point both drop during power down; therefore, a time constant circuit (R8, C4) might be added to the reference voltage input. The comparator output is fed to an input on the MC74HC373 then NANDed with the normal chip select to form $\overline{CE}$ for the RTC. The additional delay of one-clock cycle (AS) is added to improve noise sensitivity problems.

OTHER FUNCTIONS

When the main +5-volt power is removed, diode D1 is reverse-biased, diode D2 is forward biased and the battery (BBV) furnishes power to the MC146818 and other backup components. A Schottky diode is used for D1 to minimize V_{DD} potential between the system and the RTC during normal operation. Diode D2 may be selected according to the required backup battery voltage and standby operating voltage. The RTC remains in the battery backup mode until power up and the main supply reaches +9 volts. This power up point allows the MPU to stabilize before the RTC is accessed.

The $\overline{RESET}$ and PS pins of the MC146818 are also connected to the battery. These two inputs are not affected during a power shutdown unless the battery is disconnected. A logic zero, appearing at the PS pin, sets the VRT bit in register D of the RTC. Software initialization after a power up should check the valid RAM and time (VRT) bit to determine if data in the RTC is valid. Delay network R9, C7 provides the necessary delay for resetting the RTC during initial power up.

The choice of the backup battery is application dependent. System constraints applicable to the selection of the proper battery include:

1) Will the system be off for extended periods of time which requires a larger battery recharge upon power up?
2) Will the system be operating continuously requiring only a trickle charge?
3) Will battery back up only be required for emergency power outages?

A primary (no recharge) battery, such as lithium batteries, could be used in a system described by 3), whereas, a secondary (rechargeable) battery, such as nickel-cadmium, would be a better choice when constraints 1) and 2) are considered. In all cases, the V_{DD} minimum to the RTC should be above +3 volts to guarantee proper operation. In fact, the MC146818 may be operated at +3 volts in complete battery operated systems. Consult the MC146818 data sheet for +3 volts, 200 kHz bus timing and parameter specifications.

ALTERNATE CIRCUIT

An alternate circuit using a zener diode is shown in Figure 2. This circuit uses a one-volt sense into the base of an NPN transistor. Other supply voltages may be sensed by selecting the appropriate zener voltage ($V_{sense} - 1 = V_{zener}$). The circuit operates as follows: when the main power is on, a one-volt drop occurs across R3. This voltage turns on transistor Q1. The resultant low at the collector of Q1 is applied to one of the MC74HC75 transparent latch data inputs. The latch is clocked by the address strobe (AS). The power-sensing non-inverted output (Q0a) is NORed with the normal chip select, then fed back and inverted through the latch. The low $\overline{Q1a}$ latch output provides the $\overline{CE}$ signal used to select the MC146818. This signal goes high at power shutdown to deselect the MC146818. Note that two AS clocks are required to pass the transistor collector level to the MC146818.

CMOS microprocessors, such as the MC146805E2, may be directly interfaced with this circuit. The component count is minimal with just the leakage currents of the NOR gate and latch added. If this circuit is used with an NMOS MPU (i.e. V_{CC} min = 4.75 volts), then the zener should sense the unregulated power supply.

In both circuits, Figures 1 and 2, the $\overline{CE}$ combined with the derived power-sense enable may be further modified to reduce component count. When the MC146818 is memory mapped, the NAND or NOR gate can be replaced with a MC74HC138 1-of-8 demultiplexer. In this case, the power sense output (Q0a or Q1a in Figure 2) is tied to the correct enable pin on the MC74HC138. The MC74HC138 is powered by the battery and its inputs require pull-down resistors.

REFERENCES

1. Motorola MC146818 Advance Information (ADI-856-R1)
2. STATEK CX1-V data sheet
3. SEIKO DS-VT-200 data sheet
4. STATEK application note AN-0005

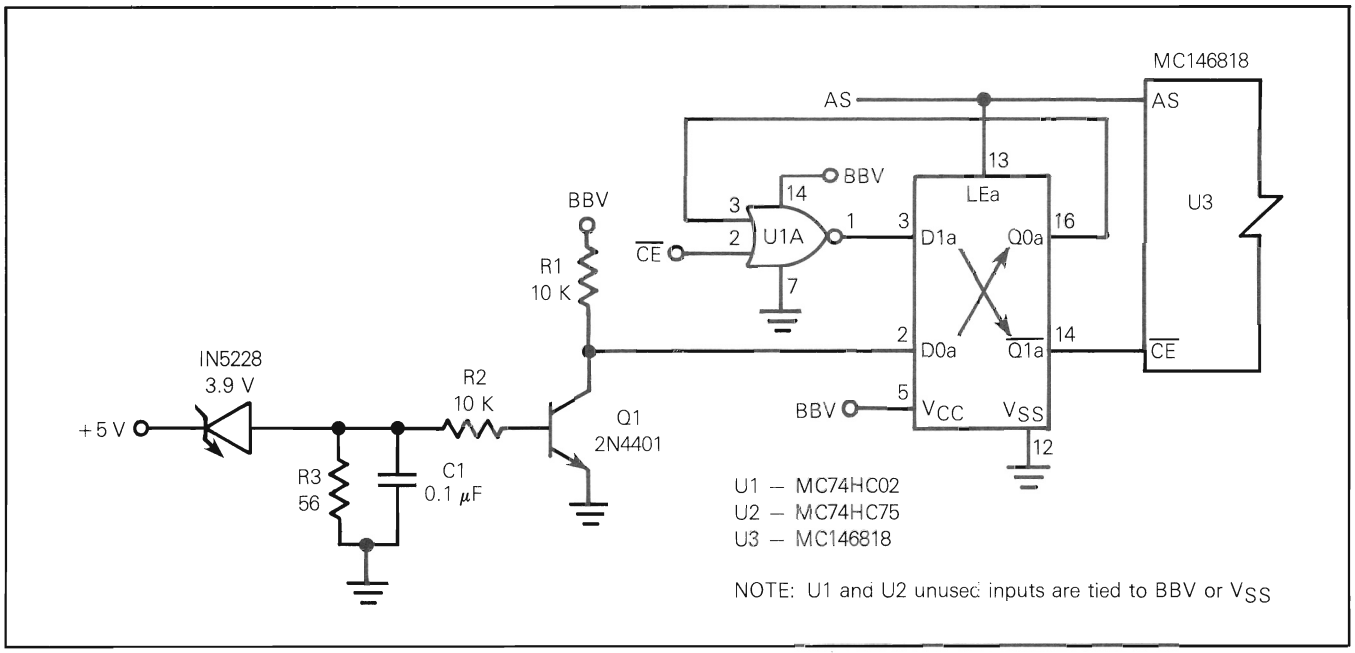

FIGURE 2 — MC146818 Battery Backup Schematic Diagram

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