

**BIDIRECTIONAL INSTRUMENTATION  
 BUS (GPIB) TRANSCEIVER**

This bidirectional bus transceiver is intended as the interface between TTL or MOS logic and the IEEE Standard Instrumentation Bus (488-1978, often referred to as GPIB). The required bus termination is internally provided.

Each driver/receiver pair forms the complete interface between the bus and an instrument. Either the driver or the receiver of each channel is enabled by its corresponding Send/Receive input with the disabled output of the pair forced to a high impedance state. An additional option allows the driver outputs to be operated in an open collector<sup>(1)</sup> or active pull-up configuration. The receivers have input hysteresis to improve noise margin, and their input loading follows the bus standard specifications.

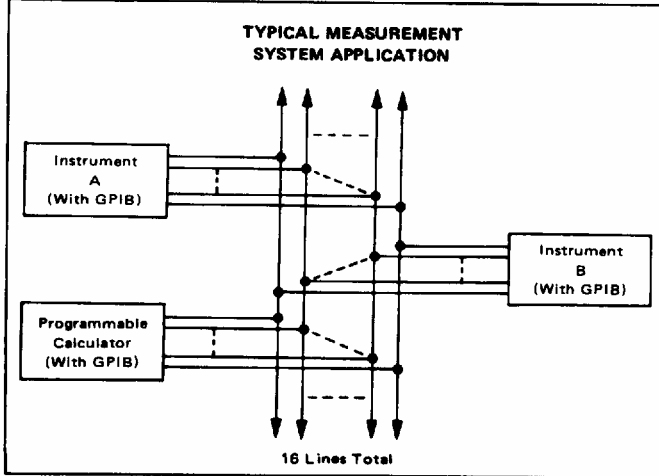
- Four Independent Driver/Receiver Pairs
- Three-State Outputs
- High Impedance Inputs
- Receiver Hysteresis — 600 mV (Typ)
- Fast Propagation Times — 15–20 ns (Typ)
- TTL Compatible Receiver Outputs
- Single +5 Volt Supply
- Open Collector Driver Output Option<sup>(1)</sup>
- Power Up/Power Down Protection  
 (No Invalid Information Transmitted to Bus)
- No Bus Loading When Power Is Removed From Device
- Terminations Provided: Termination Removed When Device is Unpowered

<sup>(1)</sup> Selection of the "Open Collector" configuration, in fact, selects an open collector device with a passive pull-up load/termination which conforms to Figure 7, IEEE 488-1978 Bus Standard.

**TRUTH TABLE**

Send/Rec.	Enable	Info. Flow	Comments
0	X	Bus → Data	—
1	1	Data → Bus	Active Pull-Up
1	0	Data → Bus	Open Col.

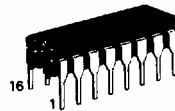
X = Don't Care



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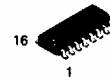
**QUAD THREE-STATE  
 BUS TRANSCEIVER WITH  
 TERMINATION NETWORKS**

**SILICON MONOLITHIC  
 INTEGRATED CIRCUIT**



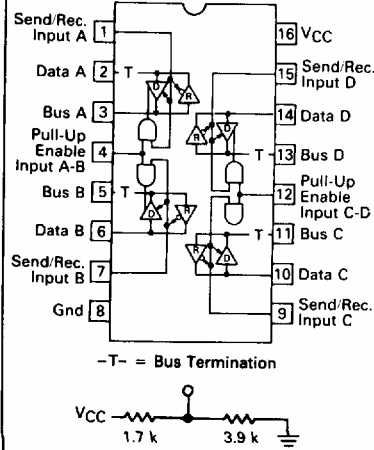
**L SUFFIX**  
 CERAMIC PACKAGE  
 CASE 620

**D SUFFIX**  
 PLASTIC PACKAGE  
 CASE 751B  
 (SO-16)



**P SUFFIX**  
 PLASTIC PACKAGE  
 CASE 648

**PIN CONNECTIONS**



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## MAXIMUM RATINGS (T<sub>A</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V <sub>CC</sub>	7.0	Vdc
Input Voltage	V <sub>I</sub>	5.5	Vdc
Driver Output Current	I <sub>O(D)</sub>	150	mA
Junction Temperature	T <sub>J</sub>	150	°C
Operating Ambient Temperature Range	T <sub>A</sub>	0 to +70	°C
Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C

## ELECTRICAL CHARACTERISTICS

(Unless otherwise noted 4.75 V ≤ V<sub>CC</sub> ≤ 5.25 V and 0 ≤ T<sub>A</sub> ≤ 70°C; typical values are at T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

Characteristic	Symbol	Min	Typ	Max	Unit
Bus Voltage (Bus Pin Open) (V <sub>I(S/R)</sub> = 0.8 V) (I <sub>I(BUS)</sub> = -12 mA)	V <sub>(BUS)</sub> V <sub>I(C)(BUS)</sub>	2.75 -	- -	3.7 -1.5	V
Bus Current (5.0 V ≤ V <sub>(BUS)</sub> ≤ 5.5 V) (V <sub>I(BUS)</sub> = 0.5 V) (V <sub>CC</sub> = 0 V, 0 V ≤ V <sub>(BUS)</sub> ≤ 2.75 V)	I <sub>(BUS)</sub>	0.7 -1.3 -	- - -	2.5 -3.2 +0.04	mA
Receiver Input Hysteresis (V <sub>I(S/R)</sub> = 0.8 V)	-	400	600	-	mV
Receiver Input Threshold (V <sub>I(S/R)</sub> = 0.8 V, Low to High) (V <sub>I(S/R)</sub> = 0.8 V, High to Low)	V <sub>ILH(R)</sub> V <sub>IHL(R)</sub>	- 0.8	1.6 1.0	1.8 -	V
Receiver Output Voltage – High Logic State (V <sub>I(S/R)</sub> = 0.8 V, I <sub>OH(R)</sub> = -800 μA, V <sub>(BUS)</sub> = 2.0 V)	V <sub>OH(R)</sub>	2.7	-	-	V
Receiver Output Voltage – Low Logic State (V <sub>I(S/R)</sub> = 0.8 V, I <sub>OL(R)</sub> = 16 mA, V <sub>(BUS)</sub> = 0.8 V)	V <sub>OL(R)</sub>	-	-	0.5	V
Receiver Output Short Circuit Current (V <sub>I(S/R)</sub> = 0.8 V, V <sub>(BUS)</sub> = 2.0 V)	I <sub>OS(R)</sub>	-15	-	-75	mA
Driver Input Voltage – High Logic State (V <sub>I(S/R)</sub> = 2.0 V)	V <sub>IH(D)</sub>	2.0	-	-	V
Driver Input Voltage – Low Logic State (V <sub>I(S/R)</sub> = 2.0 V)	V <sub>IL(D)</sub>	-	-	0.8	V
Driver Input Current – Data Pins (V <sub>I(S/R)</sub> = V <sub>I(E)</sub> = 2.0 V) (0.5 ≤ V <sub>I(D)</sub> ≤ 2.7 V) (V <sub>I(D)</sub> = 5.5 V)	I <sub>I(D)</sub> I <sub>IB(D)</sub>	-200 -	- -	40 200	μA
Input Current – Send/Receive (0.5 ≤ V <sub>I(S/R)</sub> ≤ 2.7 V) (V <sub>I(S/R)</sub> = 5.5 V)	I <sub>I(S/R)</sub> I <sub>IB(S/R)</sub>	-100 -	- -	20 100	μA
Input Current – Enable (0.5 ≤ V <sub>I(E)</sub> ≤ 2.7 V) (V <sub>I(E)</sub> = 5.5 V)	I <sub>I(E)</sub> I <sub>IB(E)</sub>	-200 -	- -	20 100	μA
Driver Input Clamp Voltage (V <sub>I(S/R)</sub> = 2.0 V, I <sub>IC(D)</sub> = -18 mA)	V <sub>IC(D)</sub>	-	-	-1.5	V
Driver Output Voltage – High Logic State (V <sub>I(S/R)</sub> = 2.0 V, V <sub>IH(D)</sub> = 2.0 V, V <sub>IH(E)</sub> = 2.0 V, I <sub>OH</sub> = -5.2 mA)	V <sub>OH(D)</sub>	2.5	-	-	V
Driver Output Voltage – Low Logic State (Note 1) (V <sub>I(S/R)</sub> = 2.0 V, I <sub>OL(D)</sub> = 48 mA)	V <sub>OL(D)</sub>	-	-	0.5	V
Output Short Circuit Current (V <sub>I(S/R)</sub> = 2.0 V, V <sub>IH(D)</sub> = 2.0 V, V <sub>IH(E)</sub> = 2.0 V)	I <sub>OS(D)</sub>	-30	-	-120	mA
Power Supply Current (Listening Mode – All Receivers On) (Talking Mode – All Drivers On)	I <sub>CCL</sub> I <sub>CCH</sub>	- -	63 106	85 125	mA

## SWITCHING CHARACTERISTICS (V<sub>CC</sub> = 5.0 V, T<sub>A</sub> = 25°C unless otherwise noted)

Propagation Delay of Driver (Output Low to High) (Output High to Low)	t <sub>PLH(D)</sub> t <sub>PHL(D)</sub>	- -	- -	15 17	ns
Propagation Delay of Receiver (Output Low to High) (Output High to Low)	t <sub>PLH(R)</sub> t <sub>PHL(R)</sub>	- -	- -	25 23	ns

NOTE 1. A modification of the IEEE 488-1978 Bus Standard changes V<sub>OL(D)</sub> from 0.4 to 0.5 V maximum to permit the use of Schottky technology.

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SWITCHING CHARACTERISTICS (continued) ( $V_{CC} = 5.0\text{ V}$ ,  $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time – Send/Receive to Data					ns
Logic High to Third State	$t_{PHZ(R)}$	–	–	30	
Third State to Logic High	$t_{PZH(R)}$	–	–	30	
Logic Low to Third State	$t_{PLZ(R)}$	–	–	30	
Third State to Logic Low	$t_{PZL(R)}$	–	–	30	
Propagation Delay Time – Send/Receive to Bus					ns
Logic High to Third State	$t_{PHZ(D)}$	–	–	30	
Third State to Logic High	$t_{PZH(D)}$	–	–	30	
Logic Low to Third State	$t_{PLZ(D)}$	–	–	30	
Third State to Logic Low	$t_{PZL(D)}$	–	–	30	
Turn-On Time – Enable to Bus					ns
Pull-Up Enable to Open Collector	$t_{POFF(E)}$	–	–	30	
Open Collector to Pull-Up Enable	$t_{PON(E)}$	–	–	20	

## PROPAGATION DELAY TEST CIRCUITS AND WAVEFORMS

FIGURE 1 – BUS INPUT TO DATA OUTPUT (RECEIVER)

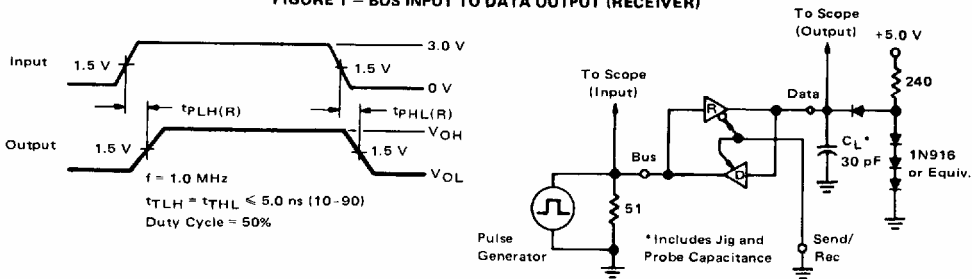


FIGURE 2 – DATA INPUT TO BUS OUTPUT (DRIVER)

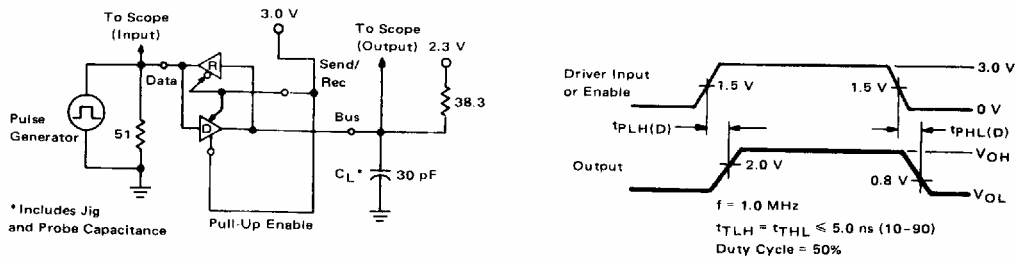


FIGURE 3 – SEND/RECEIVE INPUT TO BUS OUTPUT (DRIVER)

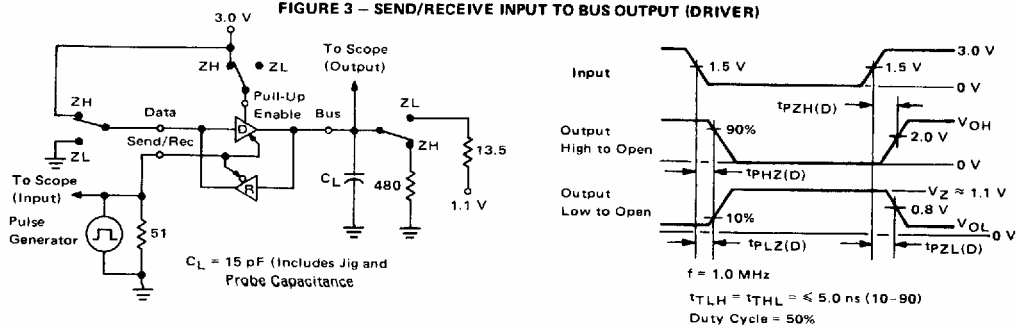


FIGURE 4 – SEND/RECEIVE INPUT TO DATA OUTPUT (RECEIVER)

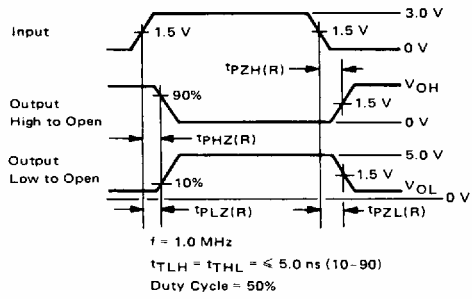
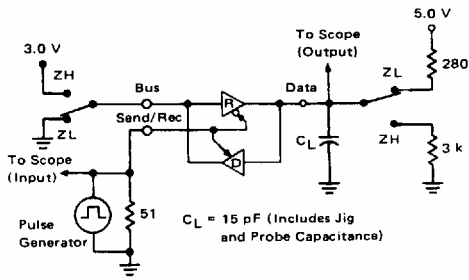


FIGURE 5 – ENABLE INPUT TO BUS OUTPUT (DRIVER)

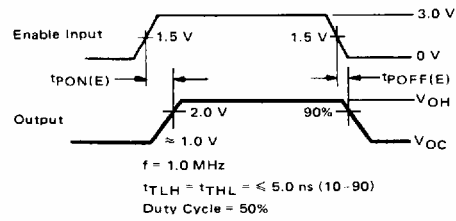
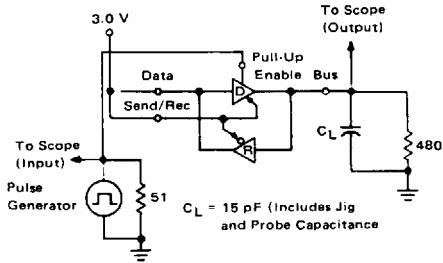


FIGURE 6 – TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS

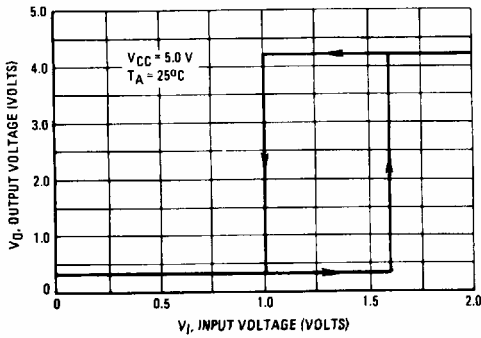
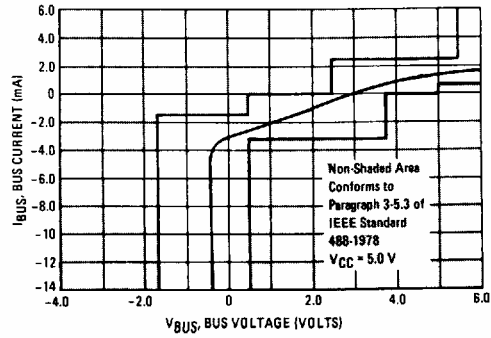
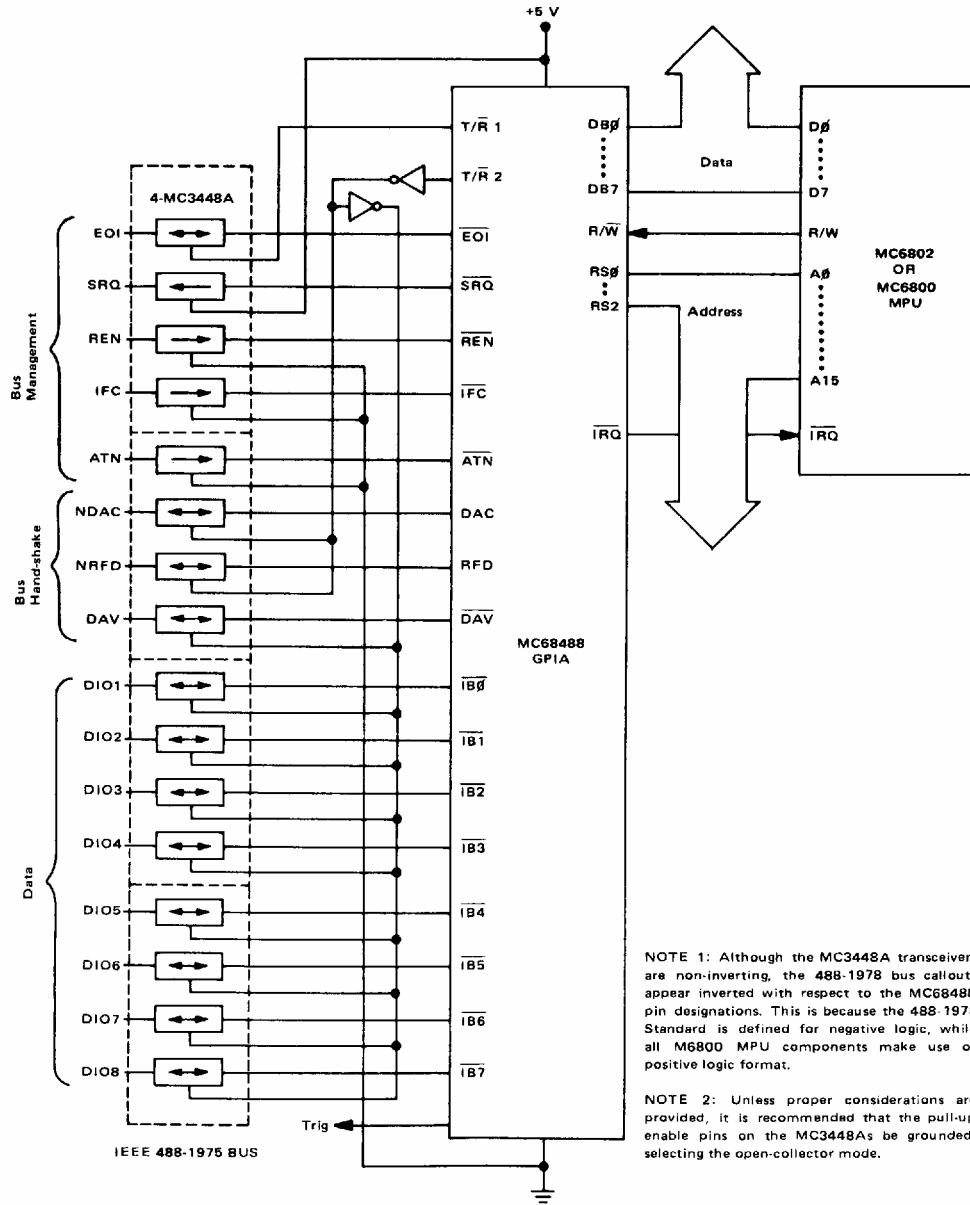


FIGURE 7 – TYPICAL BUS LOAD LINE



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FIGURE 8 - SIMPLE SYSTEM CONFIGURATION



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