

TC5517CP-15/CPL-15/CP-20/CPL-20

TC5517CF-15/CFL-15/CF-20/CFL-20

OPERATION MODE

MODE	CE	OE	H/W	$A_0 \sim A_{10}$	I/O ~ I/O _s	POWER
Read	L	L	H	Stable	Data Out	I _{DD}
Write	L	*	H	Stable	Data In	I _{DD}
Output Deselect	L	H	H	*	High Impedance	I _{DD}
** Standby	H	*	*	*	High Impedance	I _{DD}

Note : * : H or L ** : DataRetention Mode

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
V _{DD}	Power Supply Voltage	-0.3 ~ 7.0V
V _{IN}	Input Voltage	-0.3V ~ V _{DD} + 0.3V
V _{IO}	Input-Output Voltage	-0.3V ~ V _{DD} + 0.3V
P _D	Power Dissipation(Ta = 85°C)	0.8W(0.45W)*
T _{STG}	Storage Temperature	-55°C ~ 150°C
T _{OPR}	Operating Temperature	-40°C ~ 85°C
T _{SOLDER}	Soldering Temperature·Time	260°C·10sec.

*Plastic FP=0.45W

RECOMMENDED D. C. OPERATING CONDITIONS (Ta = -40 ~ 85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.2	—	V _{DD} +0.3	V
V _{IL}	Input Low Voltage	-0.3	—	0.8	V
V _{DH}	Data Retention Voltage	2.0	—	5.5	V

D. C. CHARACTERISTICS

(Ta = -40 ~ 85°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	CONDITIONS	TC5517CP-15		TC5517CP-20		UNIT		
			CF-15	CF-20	CF-15	CF-20			
I _{IL}	Input Leakage Current	0 ≤ V _{IN} ≤ V _{DD}	—	±1.0	—	±1.0	μA		
I _{LO}	I/O Leakage Current	$\overline{CE} = V_{IH}, 0V \leq V_{IO} \leq V_{DD}$	—	±5.0	—	±5.0	μA		
I _{OH}	Output High Current	V _{OH} = 2.4V	-1.0	—	-1.0	—	mA		
I _{OL}	Output Low Current	V _{OL} = 0.4V	2.0	—	2.0	—	mA		
I _{DDS1}	Standby Current	$\overline{CE} = 2 \sim 2V$	—	3.0	—	3.0	mA		
I _{DDs2}		$\overline{CE} \leq V_{DD} - 0.5V$	TC5517CPL/ CFL	Ta = 25°C	—	0.2	—	0.2	μA
				Ta = 60°C	—	1.0	—	1.0	
			TC5517CP/ CF	Ta = 25°C	—	1.0	—	1.0	
				Ta = 60°C	—	5.0	—	5.0	
I _{DDO1}	Operating Current	t _{cycle} = Min. cycle, $\overline{CE} = 0V, I_{OUT} = 0mA$	V _{IN} = V _{IH} /V _{IL}	—	45	—	30	mA	
			V _{IN} = V _{DD} /GND	—	40	—	25		
		t _{cycle} = 1μs, $\overline{CE} = 0V, I_{OUT} = 0mA$	V _{IN} = V _{IH} /V _{IL}	—	10	—	10		
			V _{IN} = V _{DD} /GND	—	5	—	5		

Note : Typical values are at Ta = 25°C, V_{DD} = 5V.

TC5517CP-15/CPL-15/CP-20/CPL-20 TC5517CF-15/CFL-15/CF-20/CFL-20

D. C. CHARACTERISTICS

(Ta = 10~60°C)

SYMBOL	PARAMETER CONDITIONS	MIN.	TYP.	MAX.	UNIT	
I_{IL}	Input Leakage Current $0V \leq V_{IN} \leq V_{DD}$	—	—	+1.0	μA	
I_{OL}	Output Leakage Current $CE = V_{DD}, 0V \leq V_{OUT} \leq V_{DD}$	—	—	+5.0	μA	
I_{OH}	Output High Current $V_{OUT} = V_{DD} - 0.2V$	—	100	—	μA	
I_{OL}	Output Low Current $V_{OUT} = 0.2V$	—	100	—	μA	
I_{BYS}	Standby Current $CE = V_{DD}$	TC5517CPL	Ta = 25°C	—	0.2	μA
		CFL	Ta = 60°C	—	1.0	
		TC5517CP	Ta = 25°C	—	1.0	
		CF	Ta = 60°C	—	5.0	
I_{DDC}	Operating Current $CE = 0V,$ $I_{OH} = 0mA$ $t_r, t_f \leq 20nsec$	$t_r = 1\mu sec$	—	2.0	3.0	mA
		$t_f = 10\mu sec$	—	0.3	0.5	

- All voltage is measured from GND.

A. C. CHARACTERISTICS

(Ta = 10~60°C, V_{DD} = 3V±10%)

Read CYCLE

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{RC}	Read Cycle Time	1000	—	—	ns
t_{ACC}	Address Access Time	—	250	1000	ns
t_{OE}	OE to Output Valid	—	80	200	ns
t_{CO}	CE to Output Valid	—	250	1000	ns
t_{COE}	CE or OE Output Active	10	—	—	ns
t_{OD}	Output High-Z Deselection	—	—	200	ns
t_{OH}	Output Hold from Address Change	20	—	—	ns

WRITE CYCLE

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{WC}	Write Cycle Time	1000	—	—	ns
t_{WP}	Write Pulse Width	500	—	—	ns
t_{AW}	Address Set up Time	100	—	—	ns
t_{WR}	Write Recovery Time	100	—	—	ns
t_{ODW}	Output High-Z from R/W	—	—	200	ns
t_{OEW}	Output Active from R/W	10	—	—	ns
t_{DS}	Data Set up Time	400	—	—	ns
t_{DH}	Data Hold Time	50	—	—	ns

A. C. TEST CONDITIONS

- Output Load : 100pF (Include Jig)
- Input Pulse Levels : 0.2V, V_{DD} - 0.2V
- Timing Measurement Level Input : 1.5V, 1.5V
- Output : 1.5V, 1.5V
- Input Pulse Rise and Fall Times : ≤20ns

TC5517CP-15/CPL-15/CP-20/CPL-20

TC5517CF-15/CFL-15/CF-20/CFL-20

Note:

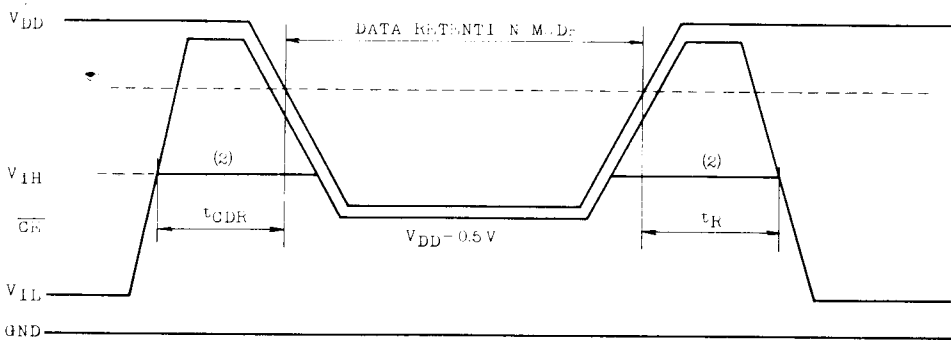
1. R/W is high for a Read Cycle.
2. $\overline{OE} = V_{IH}$ or V_{IL} . If, $\overline{OE} = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical "AND" of \overline{CE} and R/W.
 t_{WP} is measured from the latter of \overline{CE} or R/W going low to the earlier of \overline{CE} or R/W going high.
4. t_{OH} , t_{OS} are measured from the earlier of \overline{CE} or R/W going high.
5. If the \overline{CE} low transition occurs simultaneously with or later from the R/W low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
6. If the \overline{CE} high transition occurs prior to or simultaneously with the R/W high transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
7. If the R/W is low or the R/W low transition occurs prior to or simultaneously with the \overline{CE} low transition, the output buffers remain in high impedance state in this period.

DATA RETENTION CHARACTERISTICS (Ta = -40~85 C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT	
V_{DH}	Data Retention Power Supply Voltage		2.0	---	5.5	V	
I_{DDBS}	Standby Current	TC5517CPL/CFL	Ta = 25°C	---	0.005	0.2	μA
			Ta = 60°C	---	---	1.0	
		TC5517CP/CF	Ta = 25°C	---	0.05	1.0	
			Ta = 60°C	---	---	5.0	
t_{CDR}	From Chip Deselection to Data Retention Mode		0	---	---	ns	
t_R	Recovery Time		$t_{RC}(1)$	---	---		

Note:

1. t_{RC} : Read Cycle Time



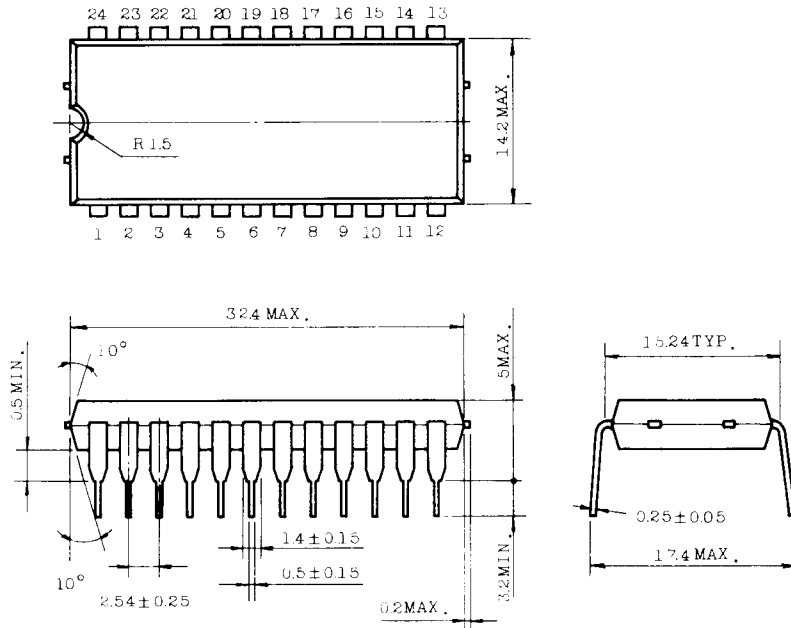
Note:

2. If the V_{IH} level of \overline{CE} is 2.2V, during the period that the V_{DD} voltage is going down from 4.5V to 2.7V I_{DDBS1} current flows.

TC5517CP-15/CPL-15/CP-20/CPL-20 TC5517CF-15/CFL-15/CF-20/CFL-20

OUTLINE DRAWINGS

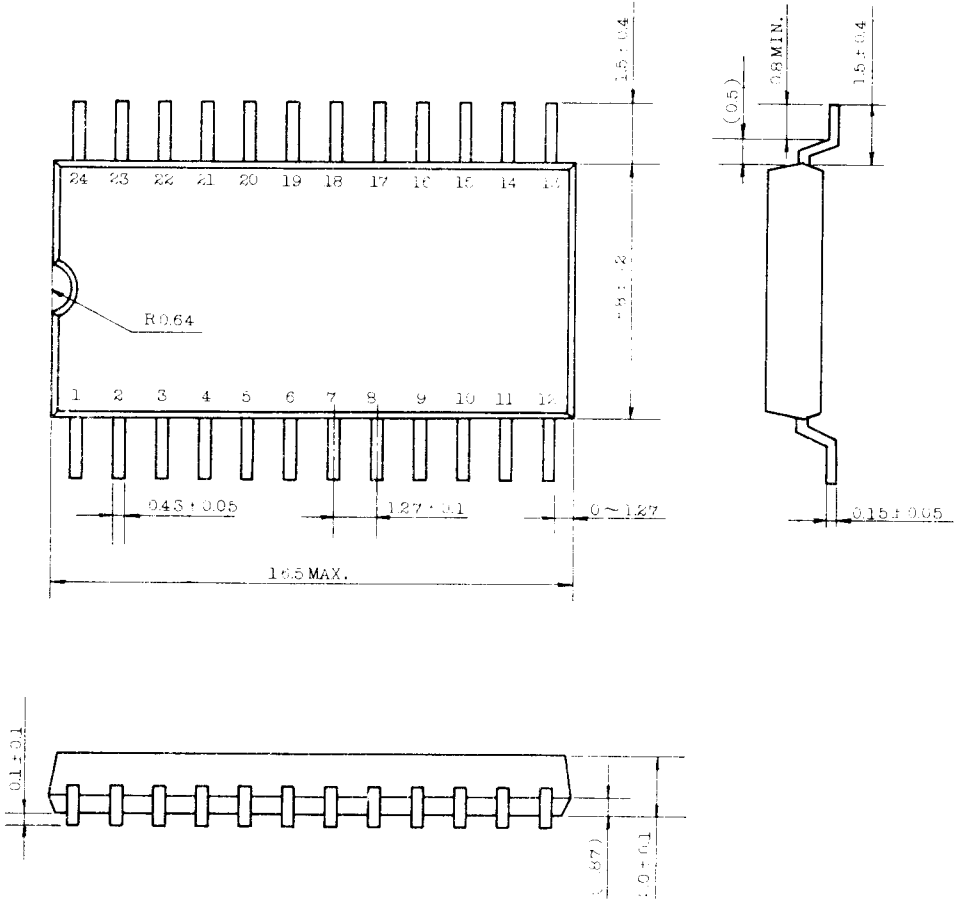
- Plastic DIP



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their longitudinal position with respect to No. 1 and No. 24 leads.
All dimensions are in millimeters.

TC5517CP-15/CPL-15/CP-20/CPL-20
TC5517CF-15/CFL-15/CF-20/CFL-20

- Plastic FP



Note : Each lead pitch is 1.27mm.
 All leads are located within 0.1mm of their true longitudinal position with respect to No. 1 and No. 24 leads.

TC5517CP-15/CPL-15/CP-20/CPL-20 TC5517CF-15/CFL-15/CF-20/CFL-20

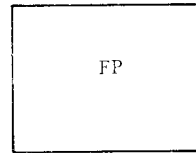
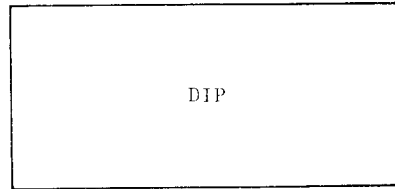
PACKAGE INFORMATION FOR FLAT PACKAGE

This new flat package is a very small and thin compared with conventional standard dual-in-line package. Differences are as follows.

1. Difference in dimension between flat and standard package.

	Flat package	Standard package
	Unit : mm	
Length	16.5	32.4
Width	9.0	14.2
Lead Pitch	1.27	2.54
Thickness	2.1	5

2. Comparison in occupied space.



3. Advantage of this package
 Small dimensions
 Capability of High Density Assembly
 Capability of thin Assembly
 Capability of Assembly on both side of PC board.

4. PC pattern layout example.

