Error correction ICs for 64-bit word sizes

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The following is a brief info on available ICs for fast 64-bit error detection and correction

1 IDT 49C460

This IC [1] is a 32-bit error detection (all single and double errors and some multiple bit errors) and correction (single errors) that uses a modified Hamming Code. Seven checkbits are used in 32-bit implementations.Two ICs can be cascaded for a 64-bit data implementation (in this case, eight ckechbits are used).

The time taken to detect and correct errors is, in the fastest version -and still preliminary- 14 ns. This time is 23 ns in 64-bit implementations (the syndrome output from the first IC is cascaded to the second one). The IC uses the same lines for both data input and output. It takes 7 ns max. to enable / disable the output buffers. The minimum cycle time is then 30 ns (estimated from the data shhet), allowing a 33 MHz operation.

Maximum throughput (64-bit, fastest IC version, preliminary) is 264 MB / s.

Package: 68-pin PLCC, PGA and Fine Pitch Flatpack. Two devices required.

2 IDT 49C465

This is a flow-thru 32-bit error detection and correction IC, cascadable for 64-bit implementations, that has the same error detection and correction capabilities as the previous IC. It is described in [2]. The minimum cycle for 64-bit cascaded operation is 56 ns.

Maximum throughput (64-bit) is ~142 MB / s.

Package: 144-pin PGA and PQFP.Two devices required.

3 IDT 49C466A

This IC [3],[4] implements a 64-bit flow-thru architecture, thus increasing the maximum throughput compared to the 49C460 and 49C465. The time taken to detect and correct errors is 15 ns and maximum clock frequency is 50 MHz.

The IC uses modified Hamming Code, with a 8-bit syndrome. Detects all single and double errors and some multi-bit errors. Corrects all single-bit errors. Additionally, generates an checks parity bits.

Maximum throughput is 400 MB / s.

Case: 208-pin PQFP. One device required.

4 IDT 49C3466

A 64-bit flow-thru 3.3V IC [5] with the same error detection and correction capabilities as the previous ones.

Maximum throughput: ~360 MB / s.

Package: 208-pin PQFP.One device required.

5 CYM7232, CYM7264 DRAM Accelerator Modules from Cypress

The CYM7232 and the CYM7264 consist of a full-function DRAM controller [6]. The CYM7232 performs 32-bit Error Detection and Correction (EDC) while CYM7264 performs 64-bit error detection and correction.

Maximum throughput (40 MHz operation, 64 bits): 320 MB / s.

References

1 IDT46C460 Data Sheet: *http://www.idt.com/docs/49C460_DS_37218.pdf*

2 IDT 46C465 dData Sheet: *http://www.idt.com/docs/49C465_DS_79711.pdf*

3 IDT46C466 Data Sheet: *http://www.idt.com/docs/49C466_DS_85314.pdf*

4 Aplication note for IDT 46C466: *http://www.idt.com/docs/49C466_AN_32976.pdf*

5 IDT 49C3466 Data Sheet: *http://www.idt.com/docs/49C3466_DS_92214.pdf*

6 *http://www.cypress.com/cypress/prodgate/modu/cym7232.html*