

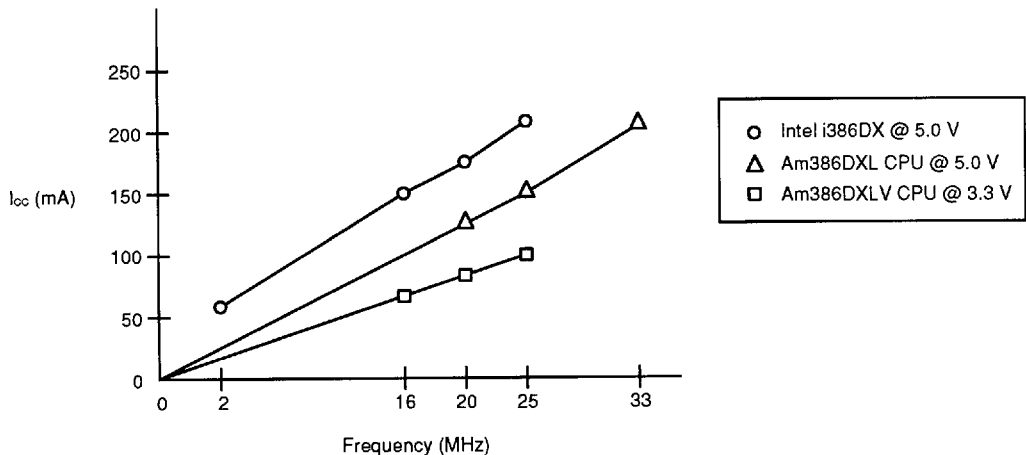


# Am386DXLV

## High-Performance, Low-Voltage, 32-Bit Microprocessor

### DISTINCTIVE CHARACTERISTICS

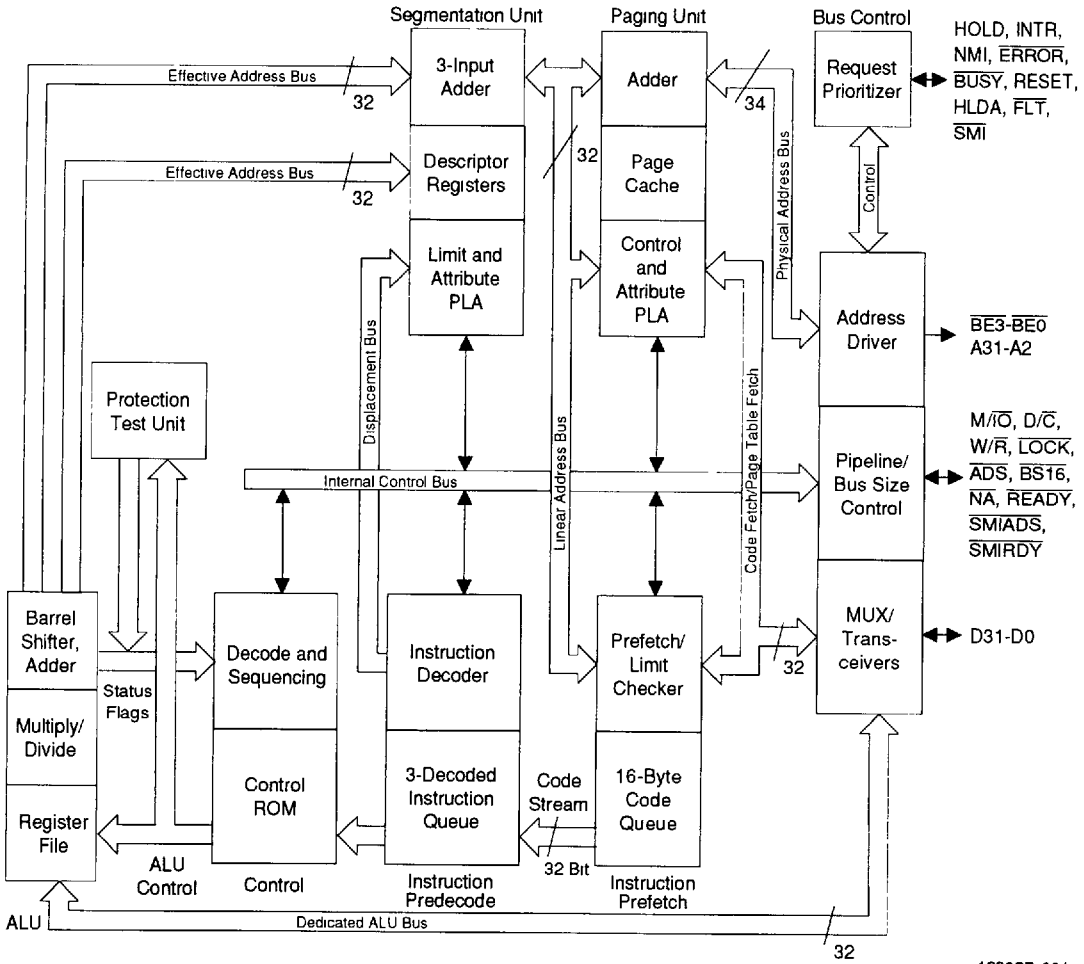
- **Operating voltage range 3.0 V to 5.5 V—Ideal for portable PC applications**
  - 25-MHz operating frequency for 3.0 V to 5.5 V
  - 33-MHz operating frequency for 4.5 V to 5.5 V
  - Twice the battery life of existing 5-V designs
  - Wide range of chipsets and other logic available for 3-V systems with support for Standby Mode operation
  - True static design for long battery life
  - Power consumption 85% lower than Intel i386DX, 65% lower than Am386DXL processor
  - Performance on demand (0 to 33 MHz)
- **SMM (System Management Mode) for system and power management**
  - SMI (System Management Interrupt) for power management independent of processor operating mode and operating system
  - SMI coupled with I/O instruction break feature provides transparent power off and auto resume of peripherals which may not be “power aware”
- SMI is non-maskable and has higher priority than Non-Maskable Interrupt (NMI)
- Automatic save and restore of the microprocessor state
- Wide range of chipsets supporting SMM available to allow product differentiation
- **Lower heat dissipation for fanless systems**
- **“Float” input to facilitate system debug and test**
- **Compatible with 386DX systems and software**
- **Supports 387DX-compatible math coprocessors**
- **132-pin PQFP package with optional protective ring for better lead coplanarity**
- **AMD® advanced 0.8 micron CMOS technology**



Note: Inputs at  $V_{cc}$  or  $V_{ss}$ .

### Typical Power Consumption

BLOCK DIAGRAM



16306B-001

## GENERAL DESCRIPTION

The Am386DXLV microprocessor is a low-voltage, true static implementation of the Intel i386DX. The operating voltage range is 3.0 V to 5.5 V. The low-voltage operation makes the Am386DXLV microprocessor ideal for both desktop and battery-powered portable personal computers. For desktop PCs, low heat dissipation allows the system designers to remove or reduce the size and cost of the system cooling fan. The Am386DXLV microprocessor operates at a maximum speed of 25 MHz from 3.0 to 5.5 V and at a maximum speed of 33 MHz from 4.5 to 5.5 V.

The Am386DXLV microprocessor's lower operating voltage and true static design enables longer battery life and/or lower weight for portable applications. At

25 MHz, this device has 80% lower operating  $I_{cc}$  than the Intel i386DX. Lowering typical operating voltage from 5.0 V to 3.3 V doubles the battery life. Standby Mode allows the Am386DXLV microprocessor to be clocked down to 0 MHz (DC) and retain full register contents. In Standby Mode, typical current draw is 0.01 mA, a greater than 1000X reduction in power consumption versus the Intel i386DX.

The Am386DXLV processor is available in a small footprint 132-pin Plastic Quad Flat Pack (PQFP) package. This surface-mount package is 40% smaller than a PGA package, allowing smaller lower-cost board designs without the need for a socket.

Additionally, the Am386DXLV processors comes with SMM for system and power management. SMI is a non-maskable, higher priority interrupt than NMI and has its own code space (1 Mb in Real Mode and 4 Gb in Protected Mode). SMI can be coupled with the I/O instruction break feature to implement transparent power management of peripherals. SMM can be used by system designers to implement system and power management code independent of the operating system or the processor mode.

The Am386DXLV processor incorporates a float pin that places all outputs in a three-state mode to facilitate board test and debug.

## FUNCTIONAL DESCRIPTION

### Benefits of Lower Operating Voltage

The Am386DXLV microprocessor has an operating voltage range of 3.0 V to 5.5 V. Low voltage allows for lower operating power consumption, longer battery life, and/or smaller batteries for notebook applications.

Because power is proportional to the square of the voltage, reduction of the supply voltage from 5.0 V to 3.3 V reduces power consumption by 56%. This directly translates to a doubling of battery life for portable applications. Lower power consumption can also be used to reduce the size and weight of the battery. Thus, 3.3-V designs facilitate a reduction in the form factor.

A lower operating voltage results in a reduction of I/O voltage swings. This reduces noise generation and provides a less hostile environment for board design. Lower operating voltage also reduces electromagnetic radiation noise, and makes FCC approval easier to obtain.

### SMM—System Management Mode

The Am386DXLV processor has a new System Management Mode (SMM) for system and power management. This mode consists of two features: System Management Interrupt (SMI) and I/O instruction break.

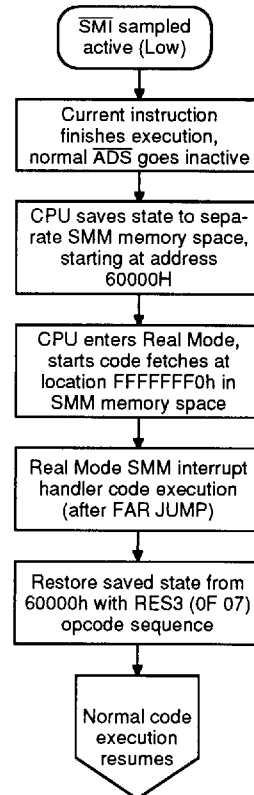
#### SMI—System Management Interrupt

SMI is implemented by using special bus interface pins. This interrupt method can be used to perform system management functions such as power management independent of processor operating mode (Real, Protected, or Virtual 8086 Modes).

SMI can also be invoked in software. This allows system software to communicate with SMI power management code. In addition, a UMOV instruction allows data transfers between SMI and normal system memory spaces.

Activating the  $\overline{\text{SMI}}$  pin invokes a sequence that saves the operating state of the processor into a separate SMM memory space, independent of the main system memory. After the state is saved, the processor is forced into Real Mode and begins execution at address FFFFFFF0h where a far jump to the SMM code is executed. This Real Mode code can perform its system

management function and then resume execution of the normal system software by executing an RES3 instruction that will reload the saved processor state and continue execution in the main system memory space. See Figure 1 for a general flowchart of an SMM operation.



16306B-002

**Figure 1. SMM Flow**

#### CPU Interface—Pin Functions

The CPU interface for SMM consists of three pins dedicated to the SMI function. One pin,  $\overline{\text{SMI}}$ , is the new interrupt input. The other two pins,  $\overline{\text{SMIADS}}$  and  $\overline{\text{SMIRDY}}$ , provide the control signals necessary for the separate SMI Mode memory space.

#### Description of SMM Operation

The execution of a System Management Interrupt has four distinct phases: the initiation of the interrupt via  $\overline{\text{SMI}}$ , a processor state save, execution of the SMM interrupt code, and a processor state restore (to resume normal operation).

#### Interrupt Initiation

A System Management Interrupt is initiated by the driving of a synchronous, active Low pulse on the  $\overline{\text{SMI}}$  pin until the first  $\overline{\text{SMIADS}}$  is asserted. This pulse period will ensure recognition of the interrupt. The CPU drives the

$\overline{\text{SMI}}$  pin active Low after the completion of the current operation (active bus cycle, instruction execution, or both). The active drive of the pin by the CPU is released at the end of the interrupt routine, following the last register read of the saved state. The CPU will drive  $\overline{\text{SMI}}$  High for two CLK2 cycles prior to releasing the drive of  $\overline{\text{SMI}}$ .

An SMI cannot be masked off by the CPU, and it will always be recognized by the CPU, regardless of operating mode. This includes the Real, Protected, and Virtual 8086 Modes of the processor.

While the CPU is in SMI Mode, a bus hold request via the HOLD pin is granted. The HLDA pin goes active after bus release and the  $\overline{\text{SMIADS}}$  pin floats along with the other pins that normally float during a bus hold cycle. The  $\overline{\text{SMI}}$  pin does not float during Bus Hold cycles.

### Processor State Save

The first set of SMM bus transfer cycles after the CPU's recognition of an active SMI is the processor saving its state to an external RAM array in a separate address space from main system memory. This is accomplished by using the  $\overline{\text{SMIADS}}$  and  $\overline{\text{SMIRDY}}$  pins for initiation and termination of bus cycles, instead of the  $\overline{\text{ADS}}$  and  $\overline{\text{READY}}$  pins. The 32-bit addresses to which the CPU saves its state are 60000H–600CBh and 60100h–60127h. These are fixed address locations for each register saved.

Pipelining must be disabled by asserting the  $\overline{\text{NA}}$  pin High in SMM. For  $\overline{\text{ADS}}$  initiated bus cycles,  $\overline{\text{BS16}}$  can be used. The value of  $\overline{\text{BS16}}$  is ignored for  $\overline{\text{SMIADS}}$  initiated bus cycles.

The save state takes approximately 630 CLK2 cycles with zero wait state memory. There are 61 data transfer cycles.

### SMI Code Execution

After the processor state is saved to the separate SMM memory space, the execution of the SMI interrupt routine code begins. The processor enters Real Mode, sets most of the register values to "reset" values (those values normally seen after a CPU reset), and begins fetching code from address FFFFFFF0h in the separate SMM memory space. Normally, the first thing the interrupt routine code does is a FAR JUMP to the Real Mode entry point for the SMI interrupt routine, which is also in SMM memory space.

INTR and NMI are disabled upon entry to SMM. See the Am386DXLV/Am386SXLV Microprocessor Technical Manual for further details on interrupts in SMM. The SMM code can be located anywhere within the 1-Mb Real Mode address space, except where the processor state is saved. I/O cycles, as a result of the IN, OUT, INS, and OUTS instructions, will go to the normal address space, utilizing the normal  $\overline{\text{ADS}}$  and  $\overline{\text{READY}}$  bus interface signals. This facilitates power management code manipulating system hardware registers as

needed through the standard I/O subsystem; a separate I/O space is not implemented.

### Processor State Restore (Resuming Normal Execution)

Returning to normal code execution in the main system memory, including restoring the processor operating mode, is accomplished by executing a RES3 (0Fh 07h) instruction. This instruction invokes a restore CPU state operation that reloads the CPU registers from the saved data in the RAM controlled by  $\overline{\text{SMIADS}}$  and  $\overline{\text{SMIRDY}}$ .

The ES:EDI register pair must point to the physical address of the saved state, this is normally at 60000h. In Real Mode, the address is calculated as  $\text{ES} \cdot 16 + \text{EDI}$ . The saved state should not cross a 64K boundary. The special opcode sequence RES3 should be executed to start the restore state operation. After completion of the restore state operation, the  $\overline{\text{SMI}}$  pin will be deactivated by the CPU and normal code execution will continue at the point where it left off before the SMI occurred.

In a zero wait state memory implementation, approximately 574 CLK2 cycles complete the restore state operation. There are 61 data transfer cycles.

### Software Features

There are several features of the SMI function that provide support for special operations during the execution of the system's software. These features involve the execution of reserved opcodes to induce specific SMI related operations.

### Software SMI Generation

Besides hardware initiation of the System Management Interrupt via the  $\overline{\text{SMI}}$  pin, there is also a software induced SMI mechanism. Generating a soft SMI involves setting a control bit 12 in Debug Register 7 (DR7) and executing an SMI instruction (reserved opcode F1h).

The functional sequence of the software-based SMI is identical to the hardware-based SMI with the exception that the  $\overline{\text{SMI}}$  pin is not initially driven active by an external source. Upon execution of a soft SMI opcode, the  $\overline{\text{SMI}}$  pin is driven active (Low) by the processor before the save state operation begins.

### Memory Transfers to Main System Memory

While executing an SMI routine, the interrupt code can initiate memory data reads and writes to the main system memory using the normal  $\overline{\text{ADS}}$  and  $\overline{\text{READY}}$  pins. This is accomplished by using reserved opcodes that are special forms of the MOV instruction (called UMOV). The UMOV opcodes can move byte, word, or double-word register operands to or from main system memory. Multiple data transfers using the normal  $\overline{\text{ADS}}$  and  $\overline{\text{READY}}$  pins will occur if the operands are misaligned relative to the effective address used. The UMOV opcodes are 0Fh 10h, 0Fh 11h, 0Fh 12h, and 0Fh 13h.

The UMOV instruction can use any of the 386 addressing modes, as specified in the ModR/M byte of the opcode. Note that the 16- and 32-bit versions are the same opcodes with the exception of the 66h operand size prefix. The BS16 line is recognized during the normal memory space data transfer(s) initiated by these instructions.

### I/O Instruction Break

The Am386DXLV processor has an I/O instruction break feature that allows the system logic to implement I/O trapping for peripheral devices. To enable the I/O instruction break feature, IIBEN must first be asserted active Low. On detecting an I/O instruction, the processor prevents the execution unit from executing further instructions until  $\overline{\text{READY}}$  is driven active Low by the system. Once  $\overline{\text{READY}}$  is driven active, the execution unit either immediately responds to any active interrupt request or continues executing instructions following the I/O instruction that caused the break.

The I/O instruction break feature can be used to allow system logic to implement I/O trapping for peripheral devices. On sensing an I/O instruction, the system drives the SMI interrupt active before driving  $\overline{\text{READY}}$  active. This ensures that the service routine is executed immediately following the I/O instruction that caused the break. (If the I/O instruction break feature is not enabled via IIBEN, several instructions that follow the I/O instruction that caused the break will execute before the SMI service routine is executed.) The SMI service routine can access the peripheral for which  $\overline{\text{SMI}}$  was asserted and modify the peripheral's state.

The SMI service routine normally returns to the instruction following the I/O instruction that caused the break. By modifying the saved state instruction pointer, the routine can choose to return to the I/O instruction that caused the break and re-execute that instruction. The default is to return to the following instruction (except for REP I/O strings). To re-execute the I/O instruction that caused the break, the SMI service routine must copy the I/O instruction pointer over the default pointer. This feature is particularly useful when an application program requests an access to a peripheral that has been powered down. The SMI service routine can restore power to the peripheral and initiate a re-execution sequence transparent to the application program. This re-execution feature should only be used if the  $\overline{\text{SMI}}$  is in response to an I/O trap with IIBEN active.

Note that the I/O instruction break feature is not enabled for memory mapped I/O devices or for 80387 bus cycles, even if IIBEN is active.

### I/O Instruction Break Timing

The I/O Instruction Break feature requires that  $\overline{\text{SMI}}$  be sampled active (Low) by the processor at least three CLK2 edges before the CLK2 edge that ends the I/O

cycle with an active  $\overline{\text{READY}}$  signal. This timing applies for both pipelined and non-pipelined cycles. If this timing constraint is not met, additional instructions may be executed by the internal execution unit prior to entering SMI Mode.

Depending on the state of the prefetch queue at the time  $\overline{\text{SMI}}$  is asserted, instruction fetch cycles may occur on the normal ADS interface before the SMI save state process begins with the assertion of  $\overline{\text{SMIADS}}$ . However, this fetched code will not be executed.

### True Static Operation

The Am386DXLV microprocessor incorporates a true static design. Unlike dynamic circuit design, the Am386DXLV device eliminates the minimum operating frequency restriction. It may be clocked from its maximum speed all the way down to 0 MHz (DC). System designers can use this feature to design true 32-bit battery-powered portable PCs with long battery life.

### Standby Mode

This true static design of the Am386DXLV microprocessor allows for a Standby Mode. At any of its operating speeds, the Am386DXLV microprocessor will retain its state (i.e., the contents of all of its registers). By shutting off the clock completely, the device enters Standby Mode. Since power consumption is a function of clock frequency, operating power consumption is reduced as the frequency is lowered. In Standby Mode, typical current draw is reduced to less than 0.01 mA at DC. This feature not only saves battery life, but it also simplifies the design of power-conscious notebook computers in the following ways.

1. Eliminates the need for software in BIOS to save and restore the contents of registers.
2. Allows simpler circuitry to control stopping of the clock since the system does not need to know the state of the processor.

### Lower Operating Icc

True static design also allows lower operating Icc when operating at any speed.

### Performance on Demand

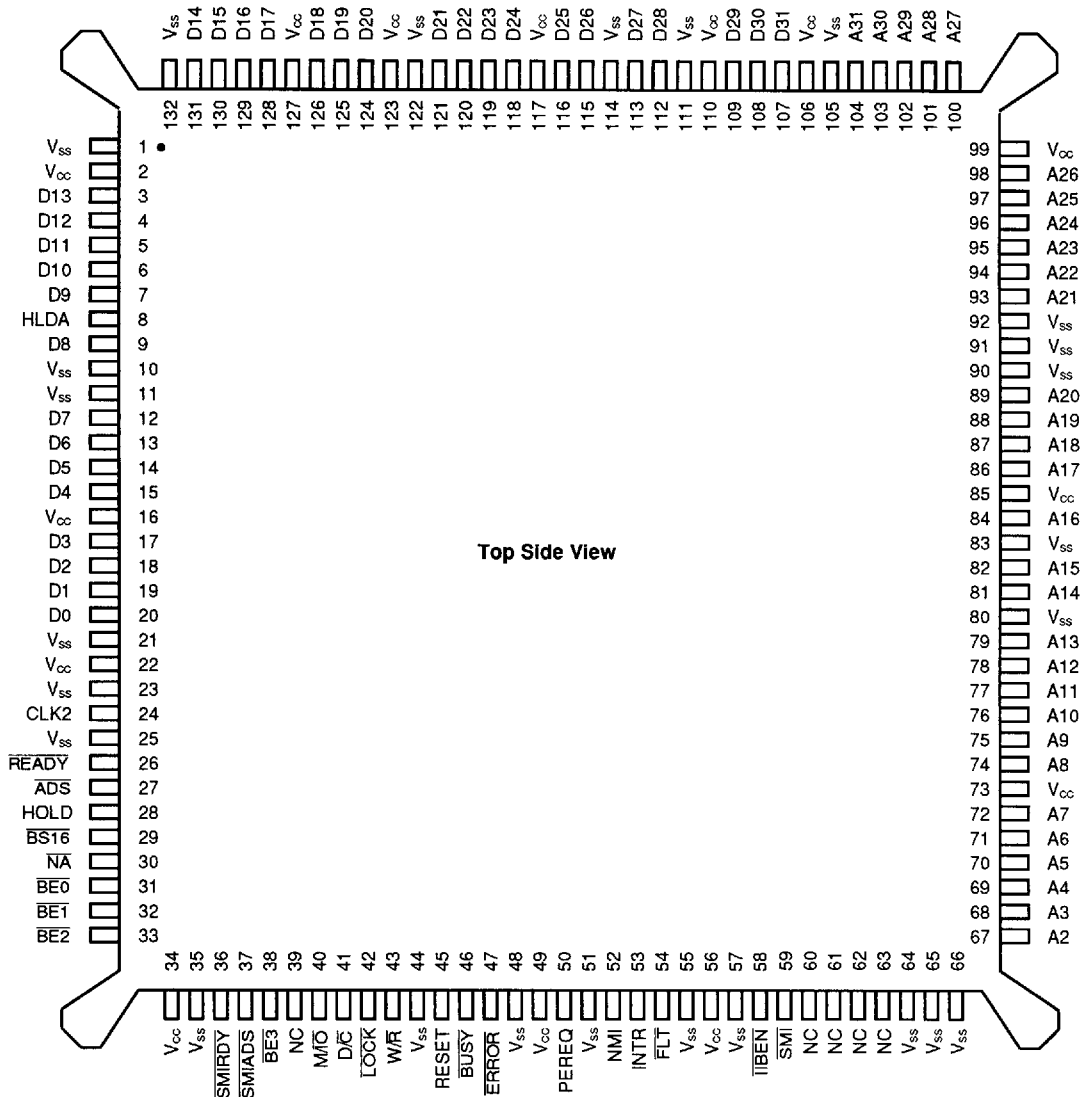
The Am386DXLV microprocessor retains its state at any speed from 0 MHz (DC) to its maximum operating speed. With this feature, system designers may vary the operating speed of the system to extend the battery life in portable systems.

For example, the system could operate at low speeds during inactivity or polling operations. However, upon interrupt, the system clock can be increased up to its maximum speed. After a user-defined time-out period, the system can be returned to a low (or 0 MHz) operating speed without losing its state. This design maximizes battery life while achieving optimal performance.

**CONNECTION DIAGRAM**

**132-Lead Plastic Quad Flat Pack (PQFP) Package — Top Side View**

**132-Pin PQFP**



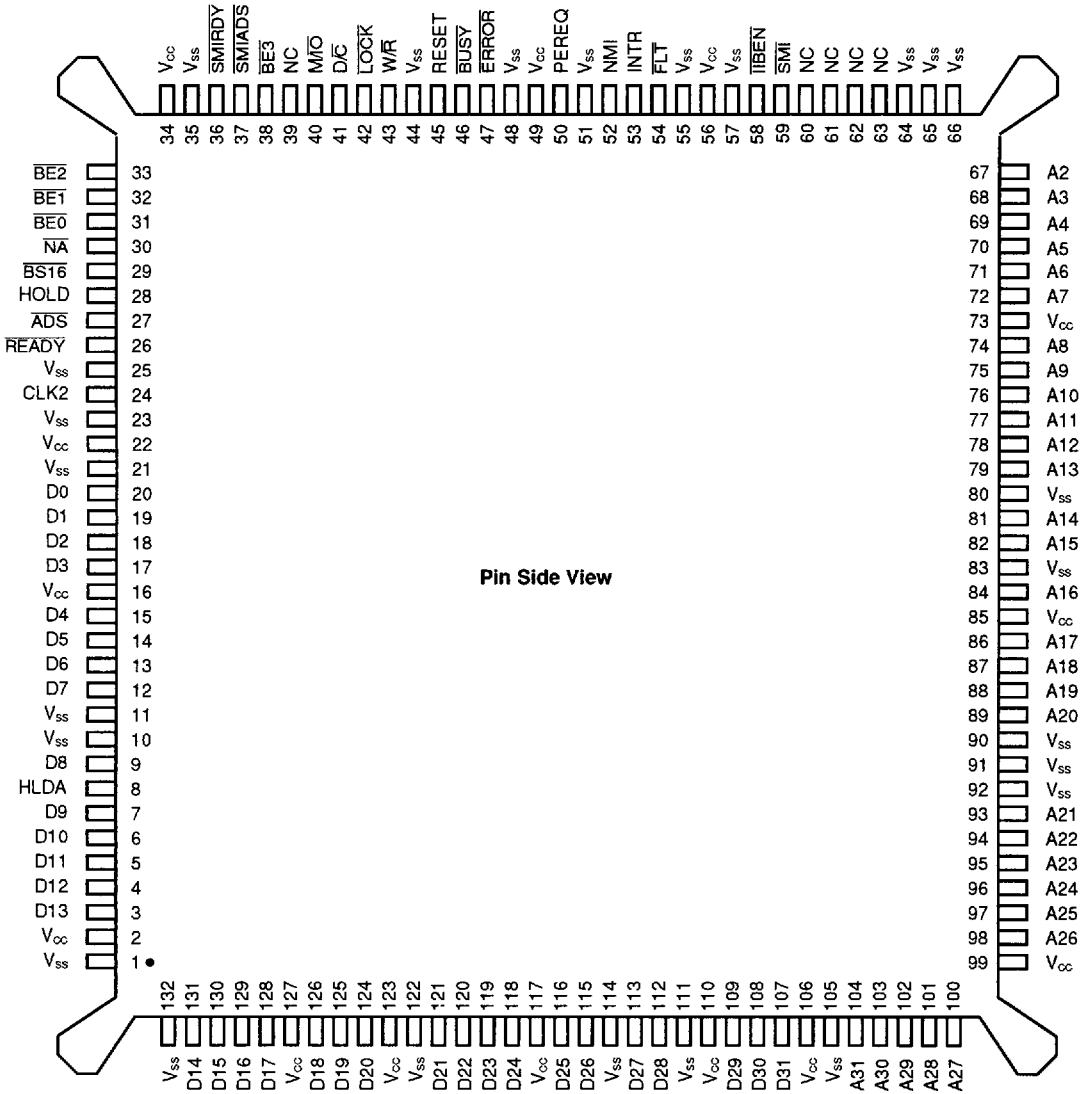
**Top Side View**

Notes. Pin 1 is marked for orientation  
 NC = Not connected, connection of an NC pin may cause a malfunction or incompatibility with future shippings of the Am386DXLV microprocessor.

**CONNECTION DIAGRAM**

**132-Lead Plastic Quad Flat Pack (PQFP) Package — Pin Side View**

**132-Pin PQFP**



Notes: Pin 1 is marked for orientation

NC = Not connected, connection of an NC pin may cause a malfunction or incompatibility with future shippings of the Am386DXLV microprocessor



**PQFP Pin Designations (Sorted by Functional Grouping)**

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
A2	67	A24	96	D6	13	D28	112	V <sub>cc</sub>	16	V <sub>ss</sub>	51
A3	68	A25	97	D7	12	D29	109		22		55
A4	69	A26	98	D8	9	D30	108		34		57
A5	70	A27	100	D9	7	D31	107		49		64
A6	71	A28	101	D10	6	D/C	41		56		65
A7	72	A29	102	D11	5	ERROR	47		73		66
A8	74	A30	103	D12	4	FLT	54		85		80
A9	75	A31	104	D13	3	HLDA	8		99		83
A10	76	ADS	27	D14	131	HOLD	28		106		90
A11	77	BE0	31	D15	130	IIBEN	58		110		91
A12	78	BE1	32	D16	129	INTR	53		117		92
A13	79	BE2	33	D17	128	LOCK	42		123		105
A14	81	BE3	38	D18	126	M/I0	40		127		111
A15	82	BS16	29	D19	125	NA	30	V <sub>ss</sub>	1		114
A16	84	BUSY	46	D20	124	NMI	52		10		122
A17	86	CLK2	24	D21	121	PEREQ	50		11		132
A18	87	D0	20	D22	120	READY	26		21	W/R	43
A19	88	D1	19	D23	119	RESET	45		23	NC	39
A20	89	D2	18	D24	118	SMI	59		25		60
A21	93	D3	17	D25	116	SMIADS	37		35		61
A22	94	D4	15	D26	115	SMIRDY	36		44		62
A23	95	D5	14	D27	113	V <sub>cc</sub>	2		48		63

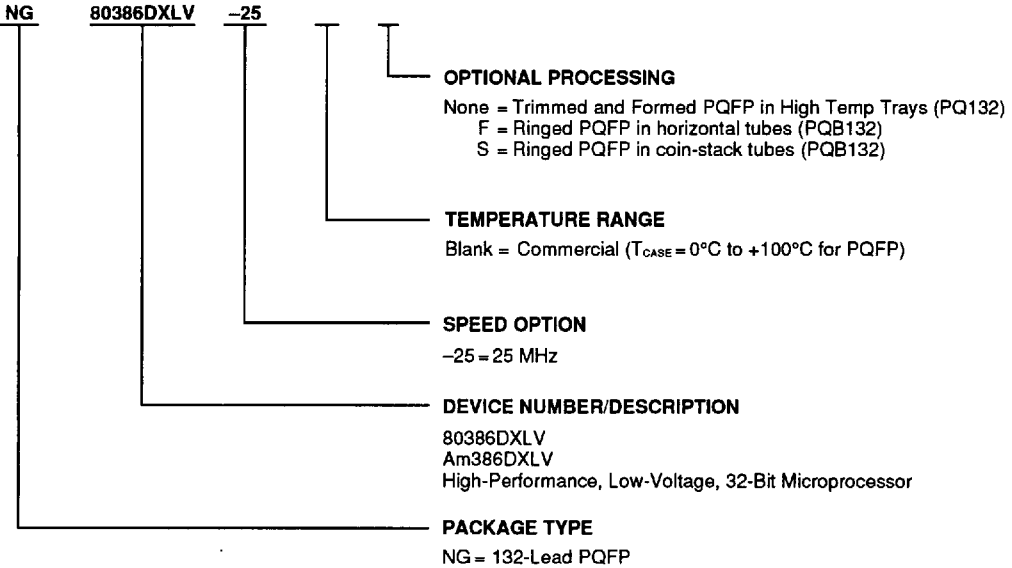
**PQFP Pin Designations (Sorted by Pin Number)**

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V <sub>ss</sub>	23	V <sub>ss</sub>	45	RESET	67	A2	89	A20	111	V <sub>ss</sub>
2	V <sub>cc</sub>	24	CLK2	46	BUSY	68	A3	90	V <sub>ss</sub>	112	D28
3	D13	25	V <sub>ss</sub>	47	ERROR	69	A4	91	V <sub>ss</sub>	113	D27
4	D12	26	READY	48	V <sub>ss</sub>	70	A5	92	V <sub>ss</sub>	114	VSS
5	D11	27	ADS	49	V <sub>cc</sub>	71	A6	93	A21	115	D26
6	D10	28	HOLD	50	PEREQ	72	A7	94	A22	116	D25
7	D9	29	BS16	51	V <sub>ss</sub>	73	V <sub>cc</sub>	95	A23	117	V <sub>cc</sub>
8	HLDA	30	NA	52	NMI	74	A8	96	A24	118	D24
9	D8	31	BE0	53	INTR	75	A9	97	A25	119	D23
10	V <sub>ss</sub>	32	BE1	54	FLT	76	A10	98	A26	120	D22
11	V <sub>ss</sub>	33	BE2	55	V <sub>ss</sub>	77	A11	99	V <sub>cc</sub>	121	D21
12	D7	34	V <sub>cc</sub>	56	V <sub>cc</sub>	78	A12	100	A27	122	V <sub>ss</sub>
13	D6	35	V <sub>ss</sub>	57	V <sub>ss</sub>	79	A13	101	A28	123	V <sub>cc</sub>
14	D5	36	SMIRDY	58	IIBEN	80	V <sub>ss</sub>	102	A29	124	D20
15	D4	37	SMIADS	59	SMI	81	A14	103	A30	125	D19
16	V <sub>cc</sub>	38	BE3	60	NC	82	A15	104	A31	126	D18
17	D3	39	NC	61	NC	83	V <sub>ss</sub>	105	V <sub>ss</sub>	127	V <sub>cc</sub>
18	D2	40	M/I0	62	NC	84	A16	106	V <sub>cc</sub>	128	D17
19	D1	41	D/C	63	NC	85	V <sub>cc</sub>	107	D31	129	D16
20	D0	42	LOCK	64	V <sub>ss</sub>	86	A17	108	D30	130	D15
21	V <sub>ss</sub>	43	W/R	65	V <sub>ss</sub>	87	A18	109	D29	131	D14
22	V <sub>cc</sub>	44	V <sub>ss</sub>	66	V <sub>ss</sub>	88	A19	110	V <sub>cc</sub>	132	V <sub>ss</sub>

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

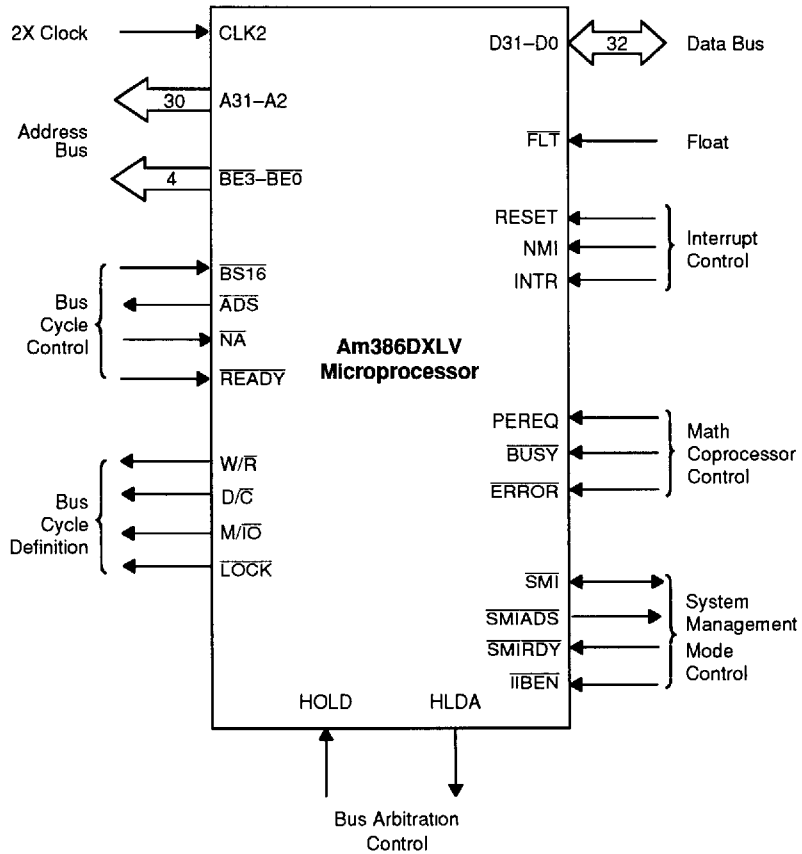


Valid Combinations		
NG	80386DXLV	-25
		-25F
		-25S

#### Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

**LOGIC SYMBOL**



15021B-003

## PIN DESCRIPTION

### A31–A2

#### Address Bus (Outputs)

Outputs physical memory or port I/O addresses.

### ADS

#### Address Status (Active Low; Output)

Indicates that a valid bus cycle definition and address (W/R, D/C, M/I $\bar{O}$ , BE3–BE0, and A31–A2) are being driven at the Am386DXLV microprocessor pins. Bus cycles initiated by ADS must be terminated by READY

### BE3–BE0

#### Byte Enable (Active Low; Outputs)

Indicates which data bytes of the data bus take part in a bus cycle.

### BS16

#### Bus Size 16 (Active Low; Input)

Allows direct connection of 32-bit and 16-bit data buses. BS16 has an internal pull-up resistor.

### BUSY

#### Busy (Active Low; Input)

Signals a busy condition from a processor extension. BUSY has an internal pull-up resistor.

### CLK2

#### Clock (Input)

Provides the fundamental timing for the Am386DXLV microprocessor.

### D31–D0

#### Data Bus (Inputs/Outputs)

Inputs data during memory, I/O, and interrupt acknowledge read cycles and outputs data during memory and I/O write cycles.

### D/C

#### Data/Control (Output)

A bus cycle definition pin that distinguishes data cycles, either memory or I/O, from control cycles (which are interrupt acknowledge, halt, and instruction fetching).

### ERROR

#### Error (Active Low; Input)

Signals an error condition from a processor extension. ERROR has an internal pull-up resistor.

### FLT

#### Float (Active Low; Input)

An input signal which forces all bidirectional and output signals, including HLDA, to the three-state condition. FLT has an internal pull-up resistor.

### HLDA

#### Bus Hold Acknowledge (Active High; Output)

Indicates that the Am386DXLV microprocessor has surrendered control of its local bus to another bus master.

### HOLD

#### Bus Hold Request (Active High; Input)

Allows another bus master to request control of the local bus.

### IIBEN

#### I/O Instruction Break Enable (Active Low; Input)

Enables the I/O instruction break feature. IIBEN has an internal pull-up resistor. Once IIBEN is driven active Low, the internal pull-up resistor is disabled until the CPU is reset.

### INTR

#### Interrupt Request (Active High; Input)

A maskable input that signals the Am386DXLV microprocessor to suspend execution of the current program and execute an interrupt acknowledge function.

### LOCK

#### Bus Lock (Active Low; Output)

A bus cycle definition pin that indicates that other system bus masters are denied access to the system bus while it is active.

### M/I $\bar{O}$

#### Memory I/O (Output)

A bus cycle definition pin that distinguishes memory cycles from input/output cycles.

### NA

#### Next Address (Active Low; Input)

Used to request address pipelining.

### NC

#### No Connect

Should always remain unconnected. Connection of an NC pin may cause the processor to malfunction or be incompatible with future steppings of the Am386DXLV microprocessor.

### NMI

#### Non-Maskable Interrupt Request (Active High; Input)

A non-maskable input that signals the Am386DXLV microprocessor to suspend execution of the current program and execute an interrupt acknowledge function.

### PEREQ

#### Processor Extension Request (Active High; Input)

Indicates that the processor extension has data to be transferred by the Am386DXLV microprocessor. PEREQ has an internal pull-down resistor.

### READY

#### Bus Ready (Active Low; Input)

Terminates the bus cycle initiated by ADS.

**RESET****Reset (Active High; Input)**

Suspends any operation in progress and places the Am386DXLV microprocessor in a known reset state.

**SMI****System Management Interrupt  
(Active Low; Input/Output)**

A Non-Maskable Interrupt (NMI) pin that signals the Am386DXLV microprocessor to suspend execution and enter System Management Mode. SMI has a dynamic pull-up resistor that is disabled when the processor is in SMM. SMI is not three-stated during hold acknowledge bus cycles.

**SMIADS****SMI Address Status (Active Low, Three-State;  
Output)**

Indicates that a valid bus cycle definition and address ( $\overline{W/\overline{R}}$ ,  $\overline{D/\overline{C}}$ ,  $\overline{M/\overline{IO}}$ ,  $\overline{BE3-\overline{BE0}}$ , and A31–A2) are being driven at the Am386DXLV microprocessor pins while in System Management Mode. Bus cycles initiated by SMIADS must be terminated by SMIRDY.

**SMIRDY****SMI Ready (Active Low; Input)**

This input terminates the current bus cycle to the SMM address space in the same manner the  $\overline{READY}$  pin does for the Normal Mode address space. SMIRDY has an internal pull-up resistor. SMIRDY must not be tied to  $\overline{READY}$ .

**V<sub>CC</sub>****System Power (Active High; Input)**

Provides the DC supply input.

**V<sub>SS</sub>****System Ground (Input)**

Provides 0-V connection from which all inputs and outputs are measured.

 **$\overline{W/\overline{R}}$** **Write/Read (Output)**

A bus cycle definition pin that distinguishes write cycles from read cycles.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . .  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$   
 Ambient Temperature Under Bias . .  $-65^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

*Stresses above those listed may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability.*

## OPERATING RANGES

Supply Voltage with Respect to  $V_{SS}$  . .  $-0.5\text{ V}$  to  $+7\text{ V}$   
 Voltage on Other Pins . . . . .  $-0.5\text{ V}$  to  $V_{CC} + 0.5\text{ V}$

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over COMMERCIAL Operating Ranges

$V_{CC} = 3.0\text{ V}$  to  $3.6\text{ V}$ ;  $T_{CASE} = 0^{\circ}\text{C}$  to  $+100^{\circ}\text{C}$

Symbol	Parameter Description	Notes	Final		Unit
			Min	Max	
$V_{IL}$	Input Low Voltage	(Note 1)	$-0.3$	$0.8$	V
$V_{IH}$	Input High Voltage		$2.0$	$V_{CC} + 0.3$	V
$V_{ILC}$	CLK2 Input Low Voltage	(Note 1)	$-0.3$	$0.8$	V
$V_{IHC}$	CLK2 Input High Voltage (25 MHz)		$2.4$	$V_{CC} + 0.3$	V
$V_{OL}$	Output Low Voltage	(Note 5)			
	$I_{OL} = 0.5\text{ mA}$ : A31–A2, D31–D0			$0.2$	V
	$I_{OL} = 0.5\text{ mA}$ : BE3–BE0, W/R, D/C, M/I $\bar{O}$ , LOCK, ADS, SMIADS, HLDA, SMI			$0.2$	V
	$I_{OL} = 2\text{ mA}$ : A31–A2, D31–D0			$0.45$	V
$V_{OH}$	Output High Voltage	(Note 5)			
	$I_{OH} = 0.1\text{ mA}$ : A31–A2, D31–D0	(Note 6)	$V_{CC} - 0.2$		V
	$I_{OH} = 0.1\text{ mA}$ : BE3–BE0, W/R, D/C, M/I $\bar{O}$ , LOCK, ADS, SMIADS, HLDA, SMI		$V_{CC} - 0.2$		V
	$I_{OH} = 0.5\text{ mA}$ : A31–A2, D31–D0		$V_{CC} - 0.45$		V
$I_{LI}$	Input Leakage Current (All pins except BS16, PEREQ, IIBEN, BUSY, FLT, ERROR, SMI, and SMIRDY)	$0\text{ V} \leq V_{IN} \leq V_{CC}$ (Note 7)		$\pm 10$	$\mu\text{A}$
$I_{IH}$	Input Leakage Current (PEREQ Pin)	$V_{IH} = V_{CC} - 0.1\text{ V}$ $V_{IH} = 2.4\text{ V}$ (Note 2)		$300$ $200$	$\mu\text{A}$
$I_{IL}$	Input Leakage Current (BS16, BUSY, FLT, ERROR, SMI, IIBEN, and SMIRDY)	$V_{IL} = 0.1\text{ V}$ $V_{IL} = 0.45\text{ V}$ (Note 3)		$-300$ $-200$	$\mu\text{A}$
$I_{LO}$	Output Leakage Current	$0.1\text{ V} \leq V_{OUT} \leq V_{CC}$		$\pm 15$	$\mu\text{A}$
$I_{CC}$	Supply Current (Note 8) CLK2 = 40 MHz: Oper. Freq. 20 MHz CLK2 = 50 MHz: Oper. Freq. 25 MHz	$V_{CC} = 3.3\text{ V}$		$V_{CC} = 3.6\text{ V}$	
		$I_{CC}$ Typ = 80		$95$	mA
		$I_{CC}$ Typ = 95		$115$	mA
$I_{CCSB}$	Standby Current (Note 8)	$I_{CCSB}$ Typ = $10\ \mu\text{A}$		$150$	$\mu\text{A}$
$C_{IN}$	Input or I/O Capacitance	$F_C = 1\text{ MHz}$ (Note 4)		$10$	pF
$C_{OUT}$	Output Capacitance	$F_C = 1\text{ MHz}$ (Note 4)		$12$	pF
$C_{CLK}$	CLK2 Capacitance	$F_C = 1\text{ MHz}$ (Note 4)		$20$	pF

- Notes: 1. The Min value,  $-0.3$ , is not 100% tested.  
 2. PEREQ input has an internal pull-down resistor  
 3. BS16, BUSY, FLT, ERROR, SMI, SMIRDY, and IIBEN inputs each have an internal pull-up resistor  
 4. Not 100% tested  
 5. Outputs are CMOS and will pull rail-to-rail if the load is not resistive  
 6.  $V_{OH}$  is only valid for SMI when exiting SMM for two CLK2 cycles  
 7. SMI and IIBEN leakage Low will be  $I_{LI}$  when pull-up is inactive and  $I_{IL}$  when pull-up is active  
 8. Inputs are at either  $V_{CC}$  or  $V_{SS}$ .

### ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature Under Bias .. -65°C to +125°C

*Stresses above those listed may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability.*

### OPERATING RANGES

Supply Voltage with Respect to  $V_{SS}$  ..... -0.5 V to +7 V  
 Voltage on Other Pins ..... -0.5 V to  $V_{CC} + 0.5$  V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

### DC CHARACTERISTICS over COMMERCIAL Operating Ranges

$V_{CC} = 3.6$  V to 5.5 V;  $T_{CASE} = 0^\circ$  C to +100°C

Symbol	Parameter Description	Notes	Final		Unit
			Min	Max	
$V_{IL}$	Input Low Voltage	(Note 1)	-0.3	0.8	V
$V_{IH}$	Input High Voltage		2.0	$V_{CC} + 0.3$	V
$V_{ILC}$	CLK2 Input Low Voltage	(Note 1)	-0.3	0.8	V
$V_{IHC}$	CLK2 Input High Voltage (33 MHz)		2.7	$V_{CC} + 0.3$	V
$V_{OL}$	Output Low Voltage $I_{OL} = 4$ mA: A31-A2, D31-D0 $I_{OL} = 5$ mA: BE3-BE0, W/R, D/C, M/I/O, LOCK, ADS, SMIADS, HLDA, SMI	(Note 5)		0.45 0.45	V V
$V_{OH}$	Output High Voltage $I_{OH} = 1$ mA: A31-A2, D31-D0 $I_{OH} = 0.9$ mA: BE3-BE0, W/R, D/C, M/I/O, LOCK, ADS, SMIADS, HLDA, SMI	(Note 5) (Note 6)	2.4 2.4		V V
$I_L$	Input Leakage Current (All pins except BS16, PEREQ, IIBEN, BUSY, FLT, SMI, SMIRDY, and ERROR)	$0 \text{ V} \leq V_{IN} \leq V_{CC}$ (Note 7)		$\pm 15$	$\mu$ A
$I_{IH}$	Input Leakage Current (PEREQ Pin)	$V_{IH} = 2.4$ V (Note 2)		200	$\mu$ A
$I_{IL}$	Input Leakage Current (BS16, BUSY, FLT, SMI, SMIRDY, IIBEN, and ERROR)	$V_{IL} = 0.45$ (Note 3)		-400	$\mu$ A
$I_{LO}$	Output Leakage Current	$0.45 \text{ V} \leq V_{OUT} \leq V_{CC}$		$\pm 15$	$\mu$ A
$I_{CC}$	Supply Current (Note 8) CLK2 = 40 MHz: Oper. Freq. 20 MHz CLK2 = 50 MHz: Oper. Freq. 25 MHz CLK2 = 66 MHz: Oper. Freq. 33 MHz	$V_{CC} = 5.0$ V $I_{CC}$ Typ = 130 $I_{CC}$ Typ = 160 $I_{CC}$ Typ = 210		$V_{CC} = 5.5$ V 155 190 245	mA mA mA
$I_{CCSB}$	Standby Current (Note 8)	$I_{CCSB}$ Typ = 20 $\mu$ A		150	$\mu$ A
$C_{IN}$	Input or I/O Capacitance	$F_C = 1$ MHz (Note 4)		10	pF
$C_{OUT}$	Output Capacitance	$F_C = 1$ MHz (Note 4)		12	pF
$C_{CLK}$	CLK2 Capacitance	$F_C = 1$ MHz (Note 4)		20	pF

- Notes
- 1 The Min value, -0.3, is not 100% tested
  - 2 PEREQ input has an internal pull-down resistor
  - 3 BS16, BUSY, FLT, ERROR, SMI, SMIRDY, and IIBEN inputs each have an internal pull-up resistor.
  4. Not 100% tested
  5. Outputs are CMOS and will pull rail-to-rail if the load is not resistive
  6.  $V_{OH}$  is only valid for SMI when exiting SMM for two CLK2 cycles
  7. SMI and IIBEN leakage Low will be  $I_L$  when pull-up is inactive and  $I_{IL}$  when pull-up is active
  - 8 Inputs are at either  $V_{CC}$  or  $V_{SS}$ .

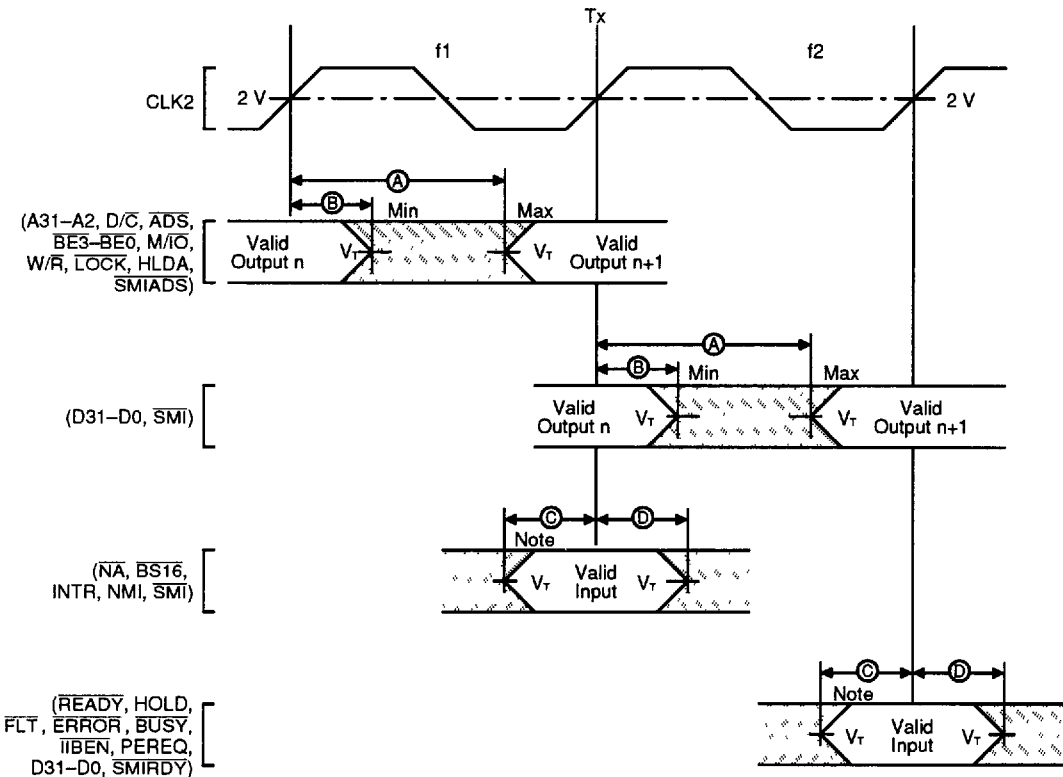
## SWITCHING CHARACTERISTICS

The switching characteristics consist of output delays, input setup requirements, and input hold requirements. All characteristics are relative to the CLK2 rising edge crossing the 2.0-V level.

Switching characteristic measurement is defined in Figure 2. Inputs must be driven to the voltage levels indicated by this diagram. Am386DXLV CPU output delays are specified with minimum and maximum limits measured as shown. The minimum Am386DXLV microprocessor delay times are hold times provided to external circuitry. Am386DXLV microprocessor input setup and hold time are specified as minimums, defining the smallest acceptable sampling window. Within the sampling

window, a synchronous input signal must be stable for correct Am386DXLV microprocessor operation.

Outputs  $\overline{W/R}$ ,  $D/\overline{C}$ ,  $M/\overline{IO}$ ,  $\overline{LOCK}$ ,  $\overline{BE3-BE0}$ ,  $\overline{ADS}$ ,  $A31-A2$ ,  $HLDA$ , and  $\overline{SMIADS}$  only change at the beginning of phase one.  $D31-D0$  (write cycles) and  $\overline{SMI}$  only change at the beginning of phase two. The  $\overline{READY}$ ,  $\overline{HOLD}$ ,  $\overline{IBEN}$ ,  $\overline{BUSY}$ ,  $\overline{ERROR}$ ,  $\overline{PEREQ}$ ,  $\overline{FLT}$ ,  $D31-D0$ , and  $\overline{SMIRDY}$  (read cycles) inputs are sampled at the beginning of phase one. The  $\overline{NA}$ ,  $\overline{BST6}$ ,  $\overline{INTR}$ ,  $\overline{NMI}$ , and  $\overline{SMI}$  inputs are sampled at the beginning of phase two.



Legend: A—Maximum Output Delay Spec  
 B—Minimum Output Delay Spec  
 C—Minimum Input Setup Spec  
 D—Minimum Input Hold Spec

Notes. 1 Input waveforms have  $t_r \leq 20$  ns from 0.8 V to 2.0 V  
 2.  $V_T = 1.0$  V at  $V_{CC} \leq 3.6$ , 1.5 V at  $V_{CC} > 3.6$ .

16306B-003

Figure 2. Drive Levels and Measurement Points



## SWITCHING CHARACTERISTICS over operating range at 25 MHz

$V_{CC} = 3.0\text{ V to }5.5\text{ V}$ ;  $T_{CASE} = 0^{\circ}\text{C to }+100^{\circ}\text{C}$

No.	Parameter Description	Notes	Ref Figures	Final		Unit
				Min	Max	
	Operating Frequency	Half of CLK2 Freq		0	25	MHz
1	CLK2 Period		4	20		ns
2	CLK2 High Time	at $V_{IHC}$	4	4		ns
3	CLK2 Low Time	at 0.8 V	4	5		ns
4	CLK2 Fall Time (Note 3)	2.4 V to 0.8 V	4		7	ns
5	CLK2 Rise Time (Note 3)	0.8 V to 2.4 V	4		7	ns
6	A31-A2 Valid Delay	$C_L = 50\text{ pF}$	3, 6	4	17	ns
7	A31-A2 Float Delay	(Note 1)	13	4	30	ns
8	BE3-BE0, LOCK Valid Delay	$C_L = 50\text{ pF}$	3, 6	4	17	ns
9	BE3-BE0, LOCK Float Delay	(Note 1)	13	4	30	ns
10	W/R, M/IO, D/C, ADS Valid Delay	$C_L = 50\text{ pF}$	3, 6	4	17	ns
10s	SMIADS Valid Delay	$C_L = 50\text{ pF}$	3, 6	4	25	ns
11	W/R, M/IO, D/C, ADS Float Delay	(Note 1)	13	4	30	ns
11s	SMIADS Float Delay	(Note 1)	13	4	30	ns
12	D31-D0 Write Data Valid Delay	$C_L = 50\text{ pF}$	6, 7	7	23	ns
12a	D31-D0 Write Data Hold Time	$C_L = 50\text{ pF}$	3, 8	2		ns
13	D31-D0 Float Delay	(Note 1)	13	4	22	ns
14	HLDA Valid Delay	$C_L = 50\text{ pF}$	3, 13	4	22	ns
14f	HLDA Float Delay	(Note 1)	14	4	30	ns
15	NA Setup Time		5	5		ns
16	NA Hold Time		5	3		ns
17	BS16 Setup Time		5	5		ns
18	BS16 Hold Time		5	3		ns
19	READY Setup Time		5	9		ns
19s	SMIRDY Setup Time		5	9		ns
20	READY Hold Time		5	4		ns
20s	SMIRDY Hold Time		5	4		ns
21	D31-D0 Read Setup Time		5	7		ns
22	D31-D0 Read Hold Time		5	5		ns
23	HOLD Setup Time		5	9		ns
24	HOLD Hold Time		5	3		ns
25	RESET Setup Time		15	8		ns
26	RESET Hold Time		15	3		ns
27	NMI, INTR Setup Time	(Note 2)	5	6		ns
27s	SMI Setup Time		5	6		ns
28	NMI, INTR Hold Time	(Note 2)	5	6		ns
28s	SMI Hold Time		5	4		ns
29	PEREQ, ERROR, BUSY, FLT, IIBEN Setup Time	(Note 2)	5	6		ns
30	PEREQ, ERROR, BUSY, FLT, IIBEN Hold Time	(Note 2)	5	5		ns
31	SMI Valid Delay		5, 13	4	22	ns
32	SMI Float Delay	(Note 1)	14	4	30	ns

- Notes
- 1 Float condition occurs when maximum output current becomes less than  $I_{LO}$  magnitude. Float delay is not 100% tested.
  - 2 These inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK2 period.
  - 3 Rise and fall times are not tested



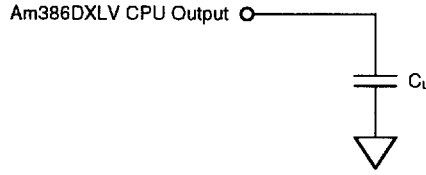
## SWITCHING CHARACTERISTICS over operating range at 33 MHz

$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ;  $T_{CASE} = 0^{\circ}\text{C to }+100^{\circ}\text{C}$

No.	Parameter Description	Notes	Ref Figures	Final		Unit
				Min	Max	
	Operating Frequency	Half of CLK2 Freq		0	33.3	MHz
1	CLK2 Period		4	15.0		ns
2	CLK2 High Time	at $V_{IHC}$	4	4.5		ns
3	CLK2 Low Time	at 0.8 V	4	4.5		ns
4	CLK2 Fall Time (Note 3)	2.4 V to 0.8 V	4		4	ns
5	CLK2 Rise Time (Note 3)	0.8 V to 2.4 V	4		4	ns
6	A31–A2 Valid Delay	$C_L = 50\text{ pF}$	3, 6	4	15	ns
7	A31–A2 Float Delay	(Note 1)	13	4	20	ns
8	$\overline{BE3}$ – $\overline{BE0}$ , $\overline{LOCK}$ Valid Delay	$C_L = 50\text{ pF}$	3, 6	4	15	ns
9	$\overline{BE3}$ – $\overline{BE0}$ , $\overline{LOCK}$ Float Delay	(Note 1)	13	4	20	ns
10	$\overline{W/R}$ , $\overline{M/\overline{O}}$ , $\overline{D/C}$ , $\overline{ADS}$ Valid Delay	$C_L = 50\text{ pF}$	3, 6	4	15	ns
10s	$\overline{SMIADS}$ Valid Delay	$C_L = 50\text{ pF}$	2, 6	4	15	ns
11	$\overline{W/R}$ , $\overline{M/\overline{O}}$ , $\overline{D/C}$ , $\overline{ADS}$ Float Delay	(Note 1)	13	4	20	ns
11s	$\overline{SMIADS}$ Float Delay	(Note 1)	13	4	20	ns
12	D31–D0 Write Data Valid Delay	$C_L = 50\text{ pF}$	6, 7	7	23	ns
12a	D31–D0 Write Data Hold Time	$C_L = 50\text{ pF}$	3, 8	2		ns
13	D31–D0 Float Delay	(Note 1)	13	4	17	ns
14	HLDA Valid Delay	$C_L = 50\text{ pF}$	3, 13	4	20	ns
14f	HLDA Float Delay	(Note 1)	14	4	20	ns
15	$\overline{NA}$ Setup Time		5	5		ns
16	$\overline{NA}$ Hold Time		5	2		ns
17	$\overline{BS16}$ Setup Time		5	5		ns
18	$\overline{BS16}$ Hold Time		5	2		ns
19	$\overline{READY}$ Setup Time		5	7		ns
19s	$\overline{SMIRDY}$ Setup Time		5	7		ns
20	$\overline{READY}$ Hold Time		5	4		ns
20s	$\overline{SMIRDY}$ Hold Time		5	4		ns
21	D31–D0 Read Setup Time		5	5		ns
22	D31–D0 Read Hold Time		5	3		ns
23	HOLD Setup Time		5	9		ns
24	HOLD Hold Time		5	2		ns
25	RESET Setup Time		15	5		ns
26	RESET Hold Time		15	2		ns
27	NMI, INTR Setup Time	(Note 2)	5	5		ns
27s	SMI Setup Time		5	5		ns
28	NMI, INTR Hold Time	(Note 2)	5	5		ns
28s	SMI Hold Time		5	4		ns
29	$\overline{PEREQ}$ , $\overline{ERROR}$ , $\overline{BUSY}$ , $\overline{FLT}$ , $\overline{IIBEN}$ Setup Time	(Note 2)	5	5		ns
30	$\overline{PEREQ}$ , $\overline{ERROR}$ , $\overline{BUSY}$ , $\overline{FLT}$ , $\overline{IIBEN}$ Hold Time	(Note 2)	5	4		ns
31	SMI Valid Delay		5, 13	4	17	ns
32	SMI Float Delay	(Note 1)	14	4	20	ns

- Notes
1. Float condition occurs when maximum output current becomes less than  $I_{LO}$  in magnitude. Float delay is not 100% tested.
  2. These inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK2 period.
  3. Rise and fall times are not tested.

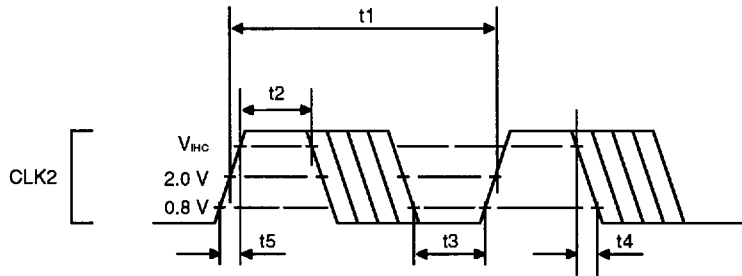
**SWITCHING CHARACTERISTICS (continued)**



$C_L$  includes all parasitic capacitances

15021B-072

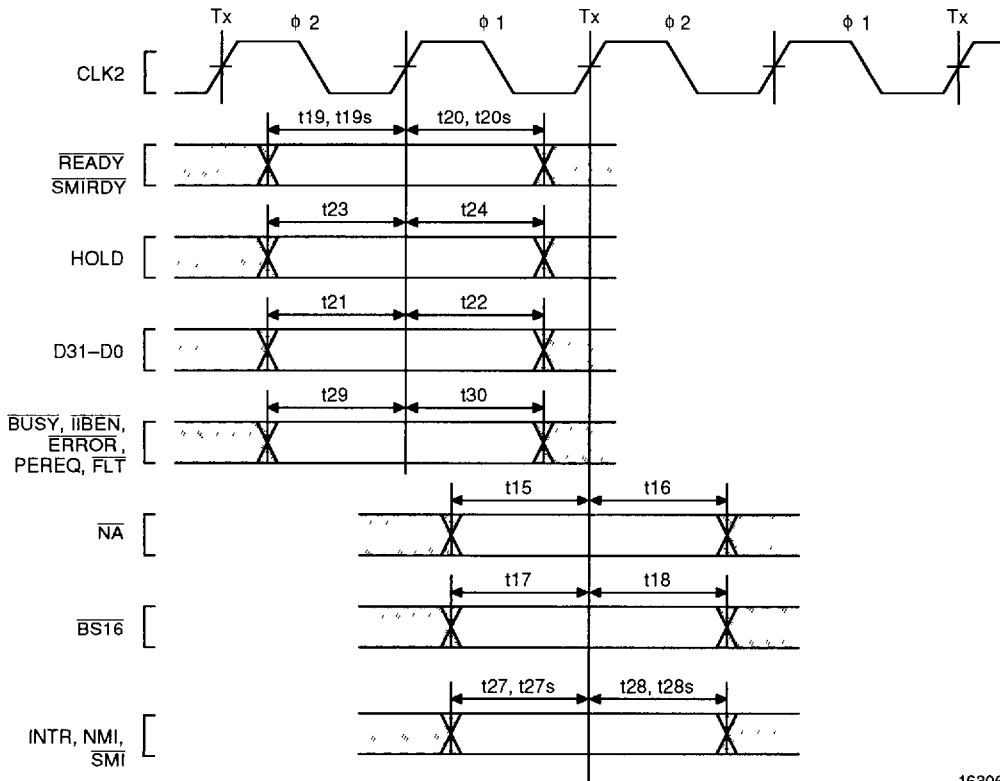
**Figure 3. AC Test Load**



**Figure 4. CLK2 Timing**

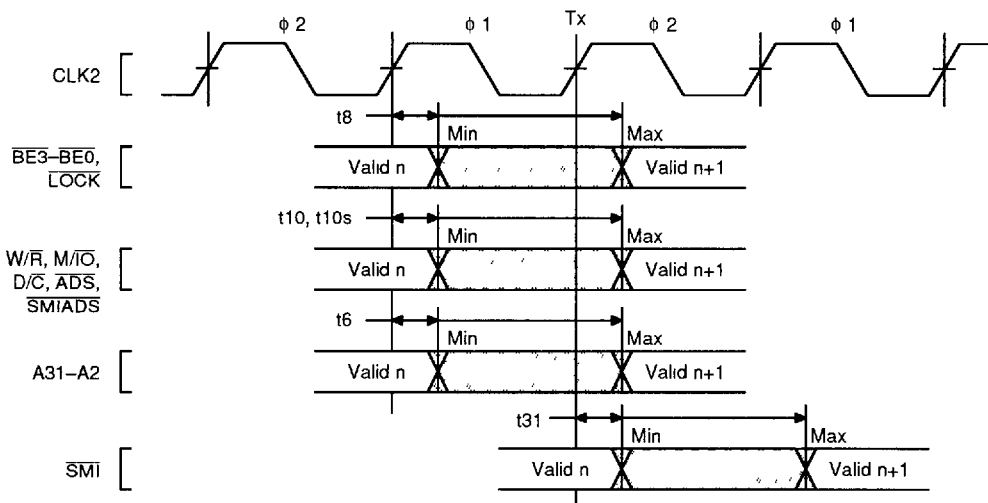
16306B-004

SWITCHING WAVEFORMS



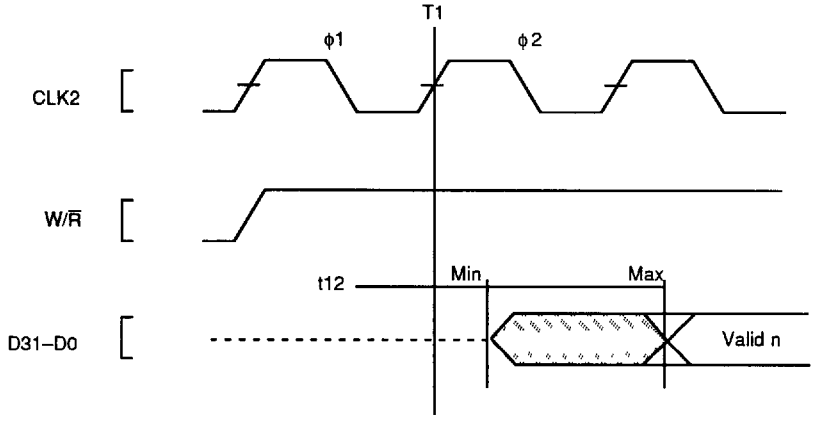
16306B-005

Figure 5. Input Setup and Hold Timing



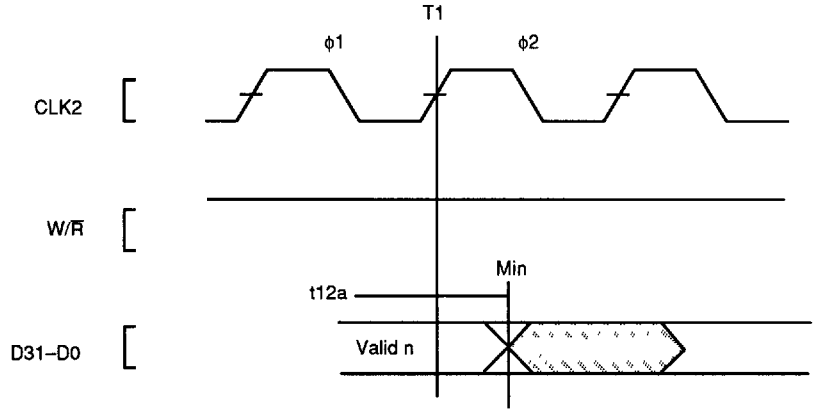
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Figure 6. Output Valid Delay Timing



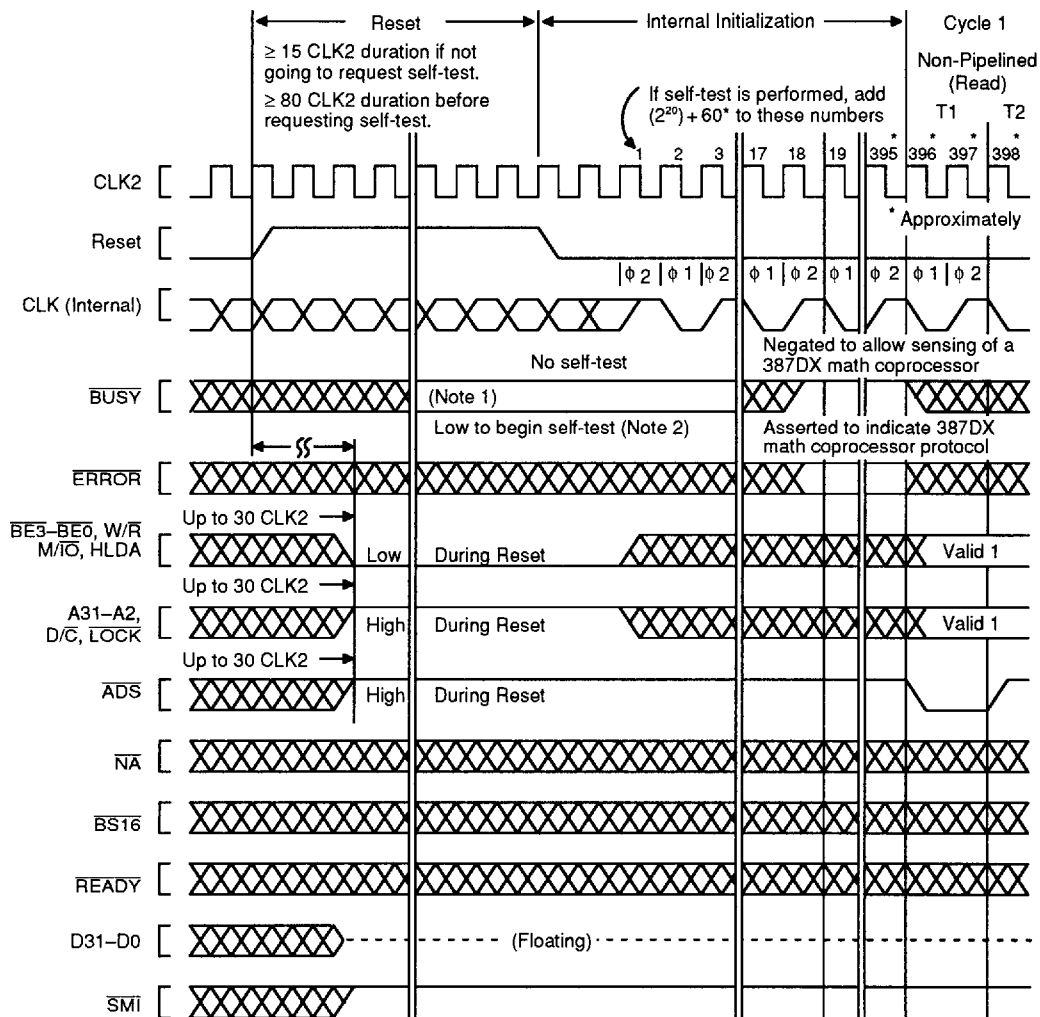
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**Figure 7. Write Data Valid Delay Timing**



15021B-077

**Figure 8. Write Data Hold Timing**



Notes 1  $\overline{BUSY}$  should be held stable for eight CLK2 periods before and after the CLK2 period in which RESET falling edge occurs  
 2 If self-test is requested, the Am386DXLV microprocessor outputs remain in their reset state as shown here

Figure 9. Bus Activity from Reset Until First Code Fetch

16306B-007

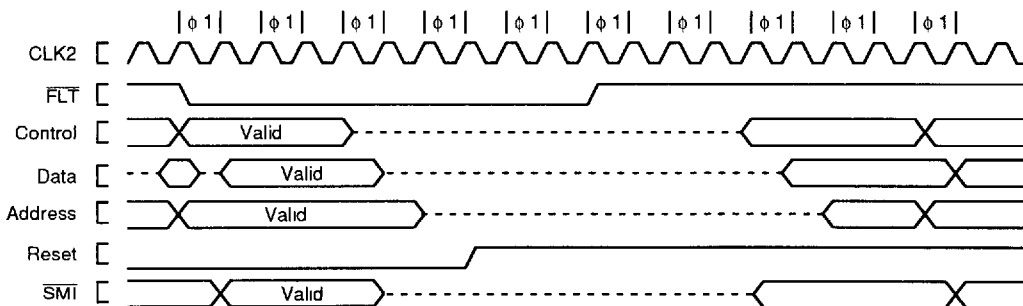
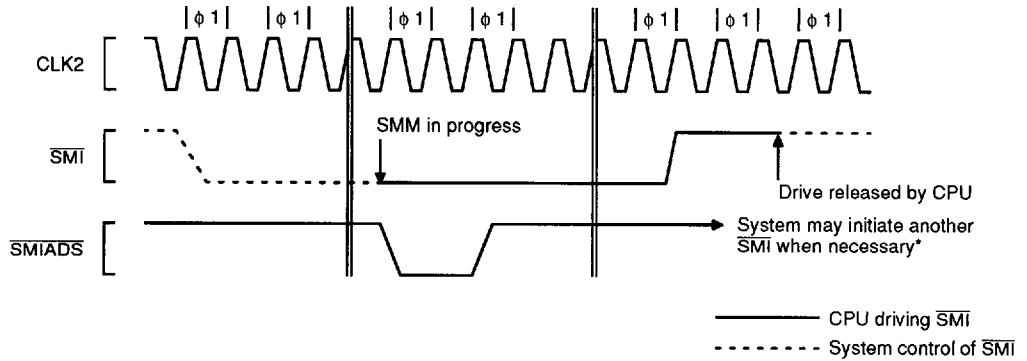


Figure 10. Entering and Exiting  $\overline{FLT}$

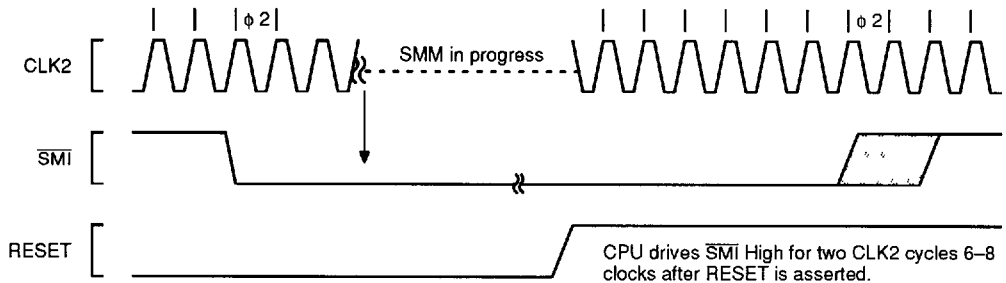
16306B-008



\*Once initiated, the system must hold  $\overline{\text{SMI}}$  Low until the first  $\overline{\text{SMIADS}}$ . At this time, the system releases control of  $\overline{\text{SMI}}$  and can not drive  $\overline{\text{SMI}}$  until three CLK2 cycles after the CPU drives  $\overline{\text{SMI}}$  High. CPU will drive  $\overline{\text{SMI}}$  High for two CLK2 cycles. The additional clock allows the CPU to completely release  $\overline{\text{SMI}}$  and prevents any driver overlap.

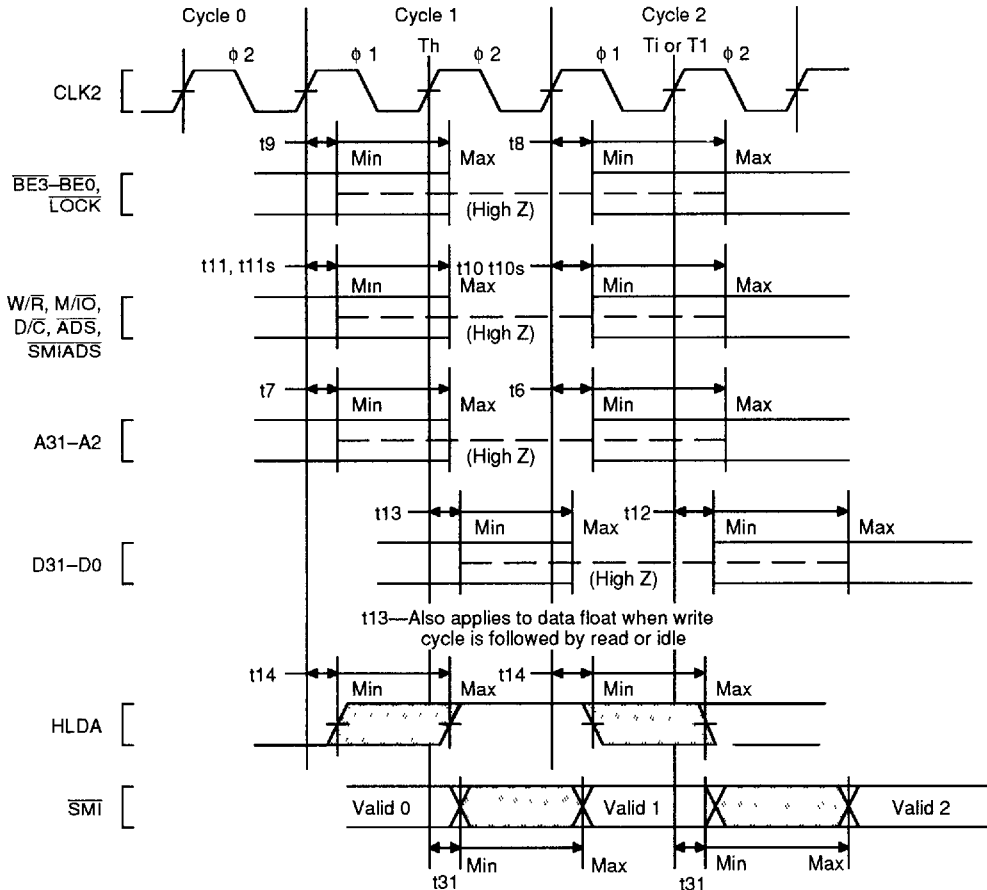
16306B-009

Figure 11. Initiating and Exiting SMM



16306B-010

Figure 12. RESET and  $\overline{\text{SMI}}$



16306B-011

Figure 13. Output Float Delay and HLDA and  $\overline{\text{SMI}}$  Valid Delay Timing



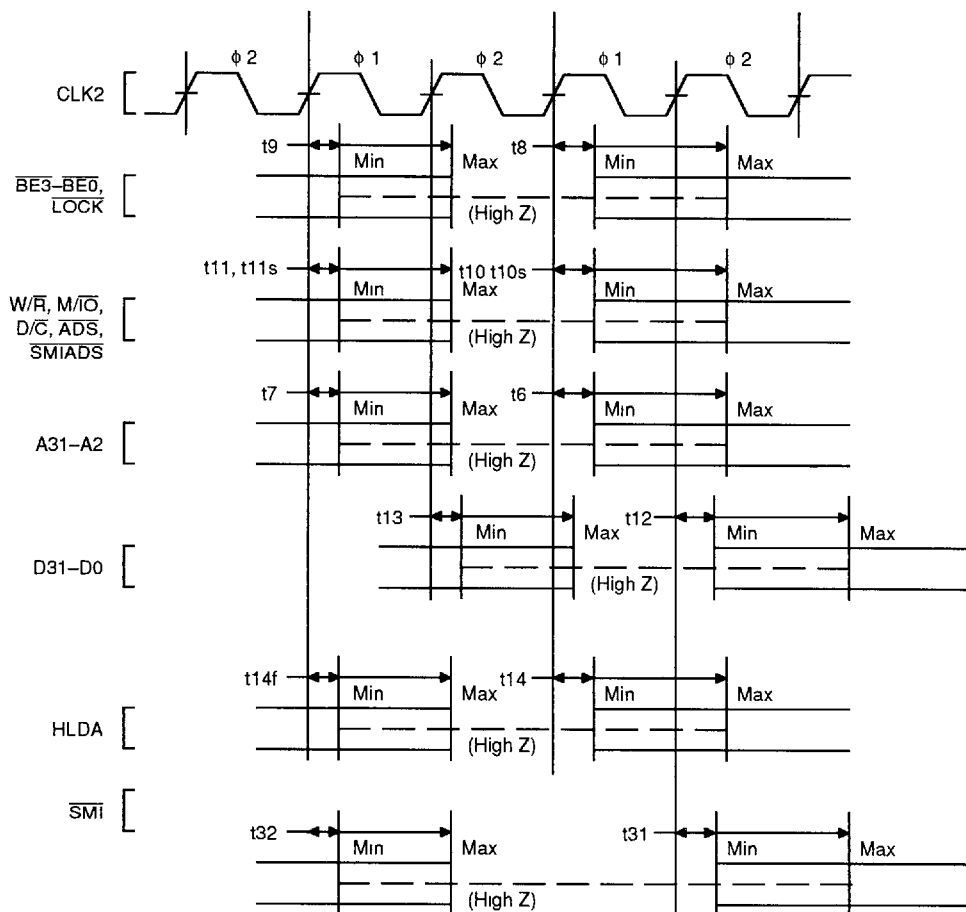
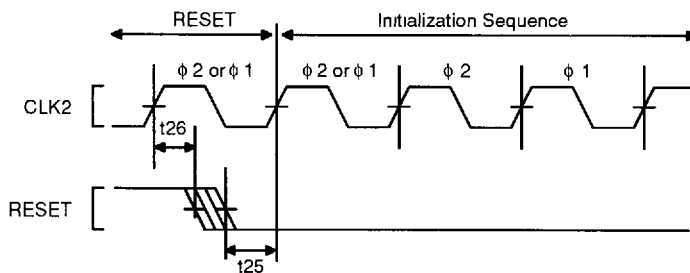


Figure 14. Output Float Delay Entering and Exiting  $\overline{\text{FLT}}$

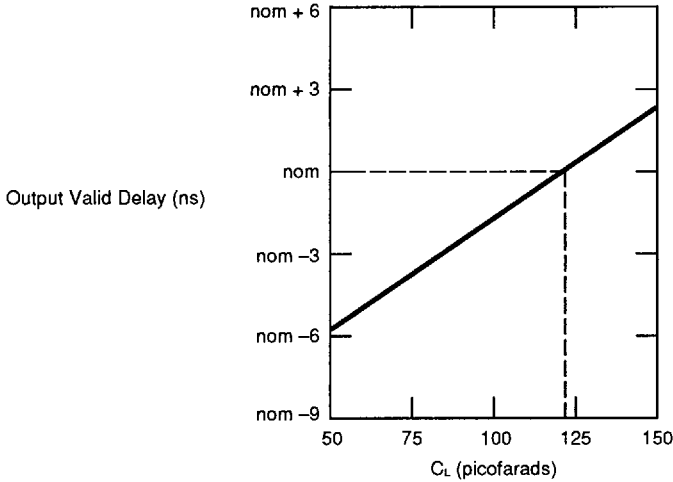
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The second internal processor phase following RESET High-to-Low transition (provided  $t_{25}$  and  $t_{26}$  are met) is  $\phi 2$

15021B-084

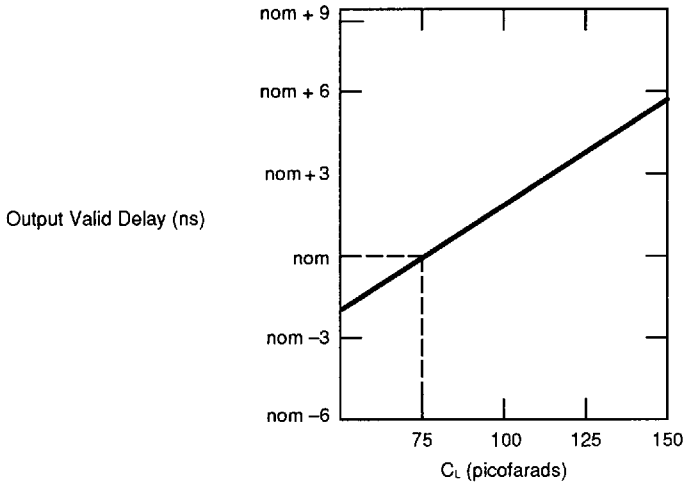
Figure 15. RESET Setup and Hold Timing and Internal Phase



Note: This graph will not be linear outside the  $C_L$  range shown

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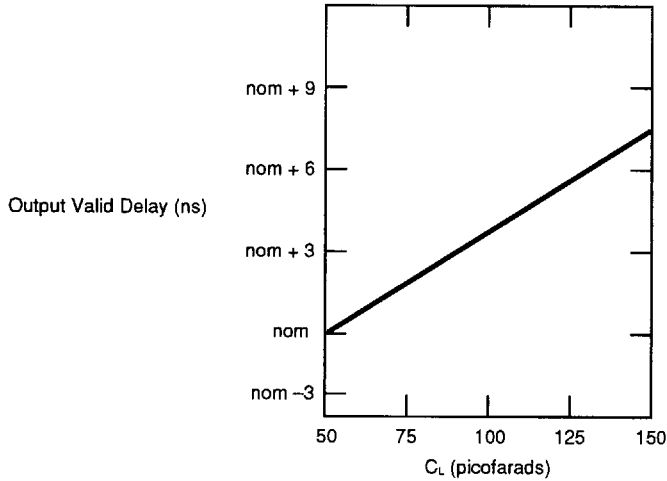
**Figure 16. Typical Output Valid Delay Versus Load Capacitance at Maximum Operating Temperature ( $C_L=120$  pF)**



Note: This graph will not be linear outside the  $C_L$  range shown.

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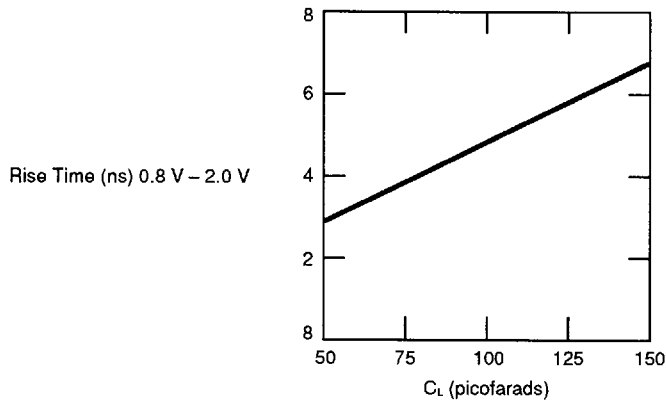
**Figure 17. Typical Output Valid Delay Versus Load Capacitance at Maximum Operating Temperature ( $C_L=75$  pF)**



Note: This graph will not be linear outside the  $C_L$  range shown

**Figure 18. Typical Output Valid Delay Versus Load Capacitance at Maximum Operating Temperature ( $C_L = 50$  pF)**

15021B-081



Note: This graph will not be linear outside the  $C_L$  range shown

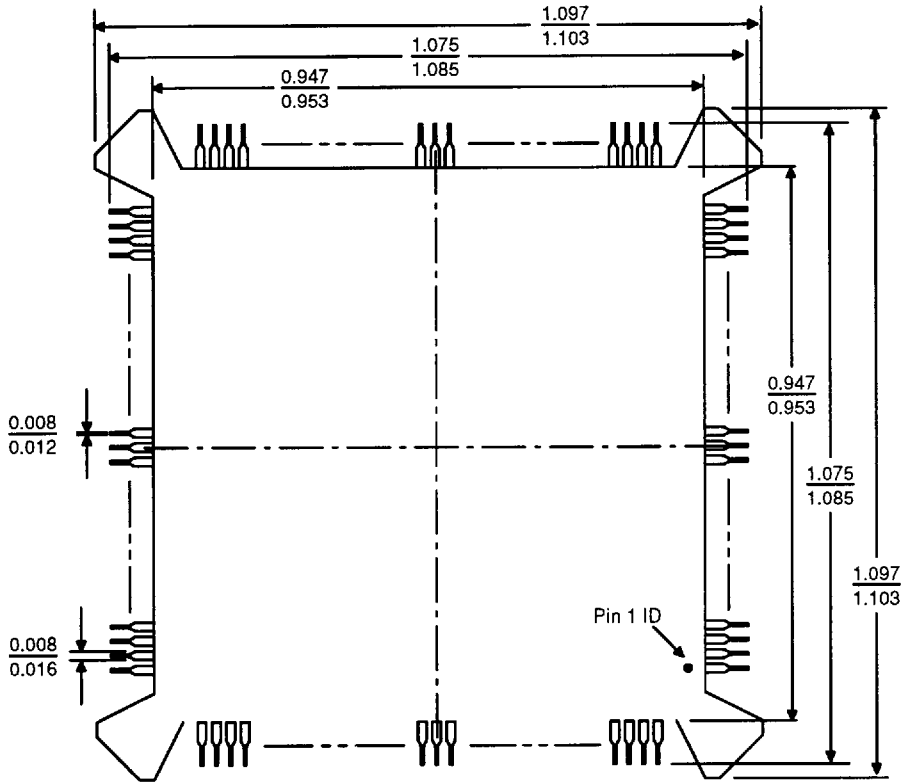
**Figure 19. Typical Output Rise Time Versus Load Capacitance at Maximum Operating Temperature**

15021B-082

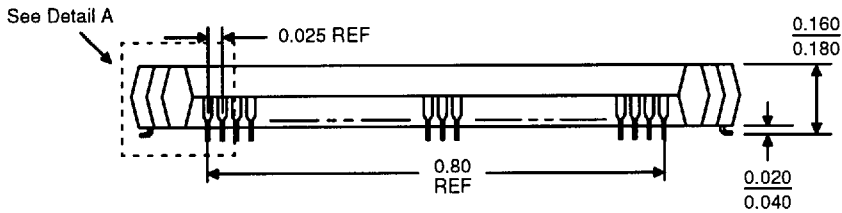
**PHYSICAL DIMENSIONS**

For reference only. All dimensions are in inches, except for the outer ring on PQB 132 which is in millimeters. BSC is an ANSI standard for Basic Space Centering.

**PQB 132 — Plastic Quad Flat Pack; Trimmed and Formed (all measurements in inches)**



**Top View**

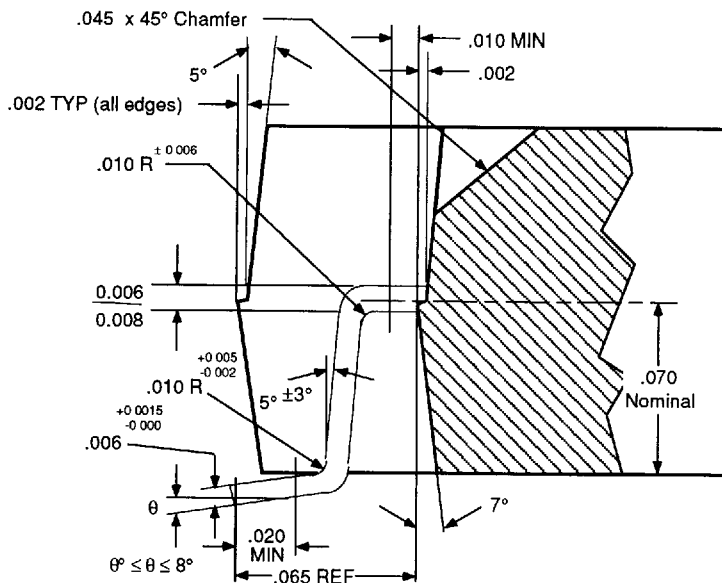


**Side View**

20011A  
CL85  
03/17/93 SG

**PHYSICAL DIMENSIONS (continued)**

**PQB 132—Plastic Quad Flat Pack; Trimmed and Formed (continued)**



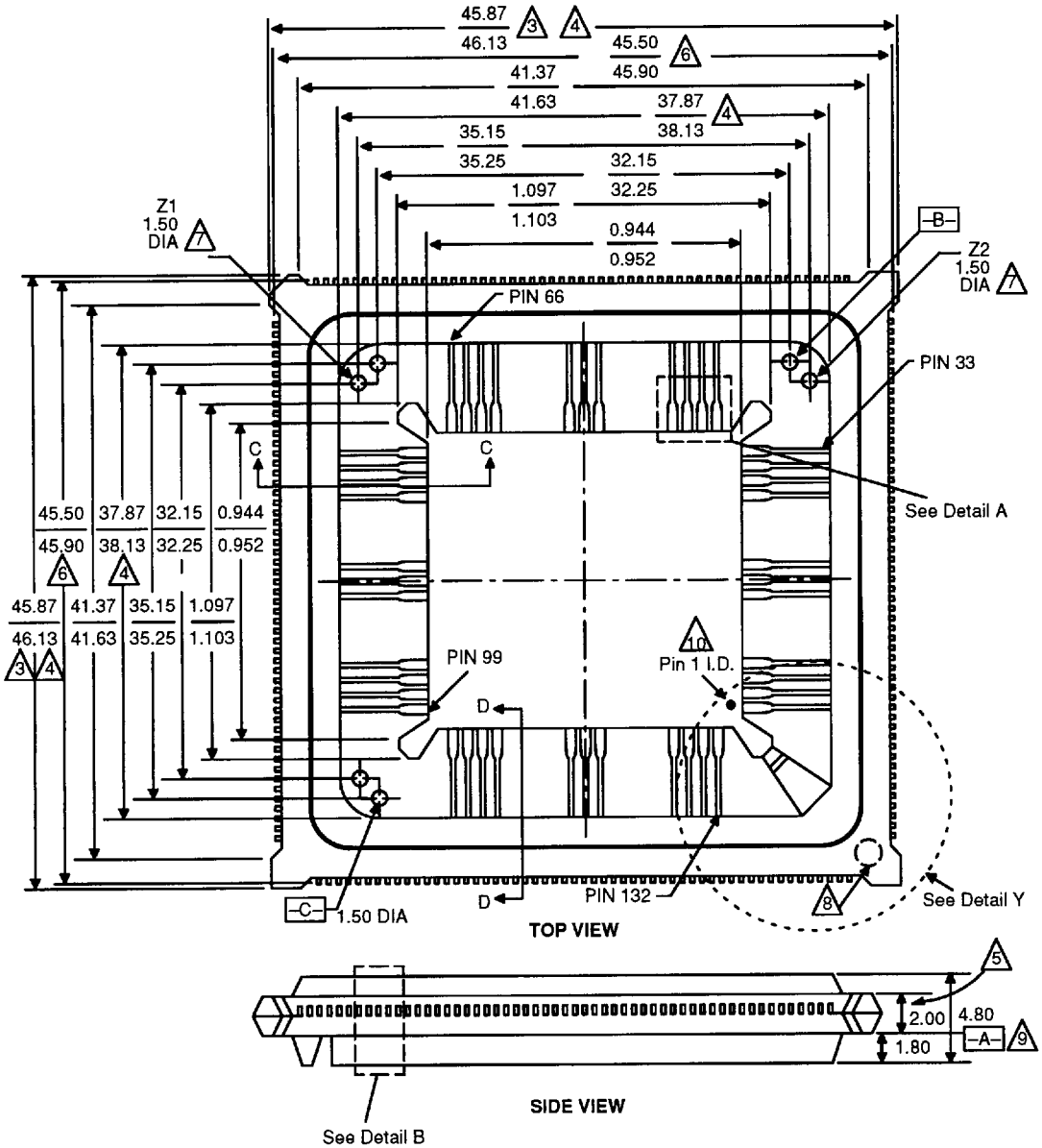
**Detail A**

**Notes:**

1. All dimensions are in inches unless otherwise specified.
2. Dimensions do not include mold protrusion.
3. Coplanarity of all leads will be within 0.004 inches measured from the seating plan. Coplanarity is measured per specification 06-500.
4. Deviation from Lead-tip true position shall be within  $\pm 0.003$  inches.
5. Half span (center of package to lead-tip) shall be within  $\pm 0.0085$  inches.

PHYSICAL DIMENSIONS (continued)

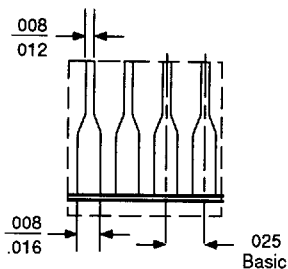
**QGB 132 — Plastic Quad Flat Pack with Molded Carrier Ring**  
 (Inner device measured in inches; outer ring measured in millimeters)



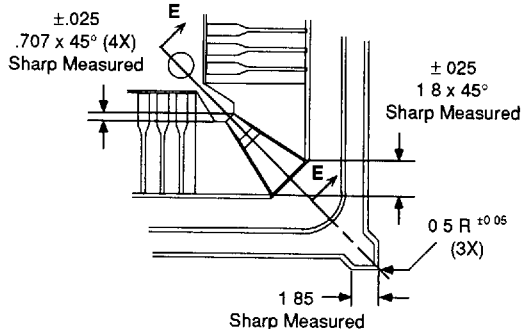
20008A  
 CJ83  
 03/17/93 SG

**PHYSICAL DIMENSIONS (continued)**

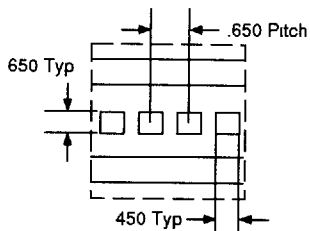
**PQB 132 — Plastic Quad Flat Pack with Molded Carrier Ring (continued)**



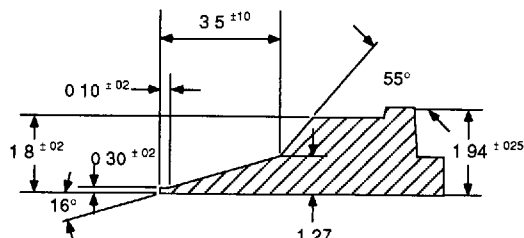
**Detail A**



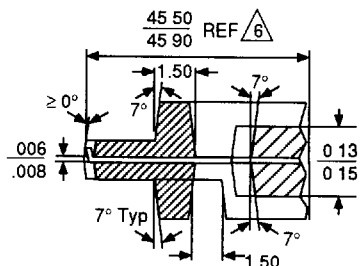
**Detail Y**



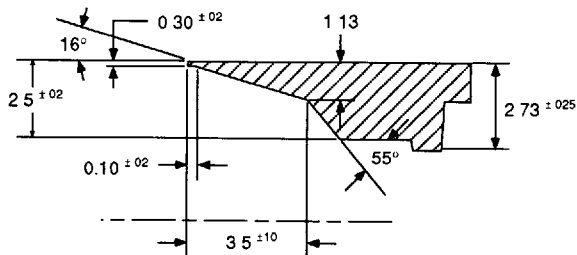
**Detail B**



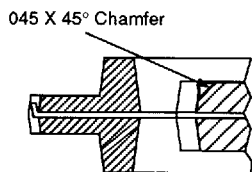
**Top Gate**



**Section C-C**



**Bottom Gate**



**Section D-D**

**Section E-E**

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**PHYSICAL DIMENSIONS (continued)****PQB 132 — Plastic Quad Flat Pack with Molded Carrier Ring****Notes:**

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Controlling dimensions: package is measured in inches and ring is measured in millimeters.
3. These dimensions do not include mold protrusion. Allowable mold protrusion is 0.2 mm per side.
4. These dimensions include mold mismatch and are measured at the parting line.
5. Dimensions are centered about centerline of lead material.
6. These dimensions are from the outside edge to the outside edge of the test points.
7. There are six locating holes in the ring. -B- and -C- datum holes are used for trim form and excise of the molded package only. Holes Z1 and Z2 are used for electrical testing only.
8. This area is reserved for vacuum pickup on each of the four corners of the ring and must be flat within 0.025 mm. No ejector pins in this area.
9. Datum -A- surface for seating in socket applications.
10. Pin one orientation with respect to carrier ring as indicated.