AMENDMENT

Am486® DX2

High-Performance, Clock-Doubled, 32-Bit Microprocessor

Advanced Micro Devices

The following should be used as additional information to corresponding sections of the current data sheet (order# 17914). The Am486DX2 microprocessor has been extended to include 66 MHz.

DISTINCTIVE CHARACTERISTICS

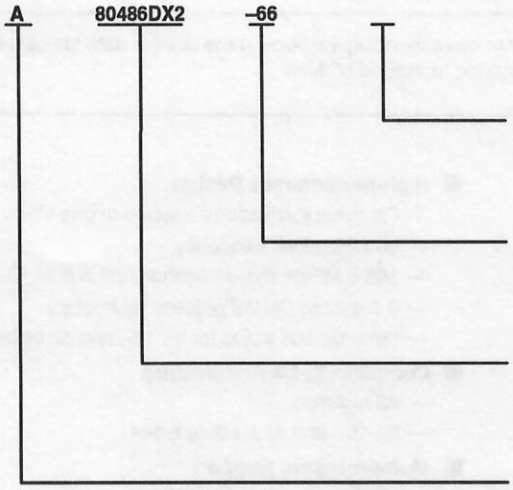
- **Binary Compatible with Large Software Base**
  - — MS-DOS, OS/2, Windows™
  - — UNIX, Windows NT™
- **High Integration On-Chip**
  - — 8-Kbyte code and data cache
  - — Paged, virtual memory management
- **Easy To Use**
  - — Built-in self test
  - — Hardware debugging support
  - — Extensive third-party software support
- **Standard 168-Pin PGA Package**
- **IEEE 1149.1 Boundary Scan Compatibility on all versions**
- **High-performance Design**
  - — Frequent instructions execute in one clock
  - — 66-MHz clock frequency
  - — 105.6 Million bytes/second burst bus at 33 MHz
  - — 0.7-micron CMOS process technology
  - — Dynamic bus sizing for 8-, 16-, and 32-bit buses
- **Complete 32-bit Architecture**
  - — All registers
  - — 8-, 16-, and 32-bit data types
- **Multiprocessor Support**
  - — Multiprocessor instructions
  - — Cache consistency
  - — Support for second-level cache
- **Pin-for-Pin Replacement of the i486DX**

Publication# 17914 Rev. A Amendment /3
Issue Date: May 1994

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



TEMPERATURE RANGE
Blank = Commercial (T_{CASE} = 0°C to +85°C)

SPEED OPTION
–66 = 66 MHz

DEVICE NUMBER/DESCRIPTION
80486DX2
Am486DX2 High-Performance, 32-Bit Microprocessor

PACKAGE TYPE
A = 168-Pin PGA (Pin Grid Array)

Valid Combinations		
A	80486DX2	–66

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ABSOLUTE MAXIMUM RATINGS

Case Temperature under Bias .... −65°C to +110°C
Storage Temperature ..... −65°C to +150°C
Voltage on any pin
with respect to ground ..... −0.5 V to V_{CC} + 0.5 V
Supply voltage with
respect to V_{SS} ..... −0.5 V to +6.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

T_{CASE} ..... 0°C to +85°C
V_{CC} ..... 5 V ± 5%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges

V_{CC} = 5 V ± 5%; T_{CASE} = 0°C to + 85°C

Symbol	Parameter	Preliminary		Unit	Notes
		Min	Max		
V_{IL}	Input Low Voltage	−0.3	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.3	V	
V_{OL}	Output Low Voltage		0.45	V	Note 1
V_{OH}	Output High Voltage	2.4		V	Note 2
I_{CC}	Power Supply Current (66 MHz)		1200	mA	Note 3
I_{CCF}	Power Supply Current in Power Down Mode		50	mA	Note 8
I_{LI}	Input Leakage Current		±15	µA	Note 4
I_{IH}	Input Leakage Current		200	µA	Note 5
I_{IL}	Input Leakage Current		−400	µA	Note 6
I_{LO}	Output Leakage Current		±15	µA	
C_{IN}	Input Capacitance (66 MHz)		13	pF	F_C = 1 MHz (Note 7)
C_O	I/O or Output Capacitance (66 MHz)		17	pF	F_C = 1 MHz (Note 7)
C_{CLK}	CLK Capacitance (66 MHz)		15	pF	F_C = 1 MHz (Note 7)

Notes:

1. *This parameter is measured at:*
   Address, Data, $\overline{BE}$n 4.0 mA
   Definition, Control 5.0 mA
2. *This parameter is measured at:*
   Address, Data, $\overline{BE}$n −1.0 mA
   Definition, Control −0.9 mA
3. *Typical supply current*
   1050 mA @ 66 MHz
4. *This parameter is for inputs without internal pull-ups or pull-downs and $0 \le V_{IN} \le V_{CC}$.*
5. *This parameter is for inputs with internal pull-downs and V_{IH} = 2.4 V.*
6. *This parameter is for inputs with internal pull-ups and V_{IL} = 0.45 V.*
7. *Not 100% tested.*
8. *The I_{CCF} specification is a target value for current requirements when the $\overline{UP}$ input is active, that is, when the Am486DX is used with an OverDrive Processor. It has not been tested.*

Switching Characteristics at 66 MHz

V_{CC} = 5 V ±5%; T_{CASE} = 0°C to + 85°C; C_L = see Note 2

Symbol	Parameter	Preliminary		Unit	Figure	Notes
		Min	Max			
	Frequency	8	33	MHz		1X Clock to Am486 CPU
t_1	CLK Period	30	125	ns	Figure 1	
t_{1a}	CLK Period Stability		0.1%	Δ		Adjacent Clocks
t_2	CLK High Time	11		ns	Figure 1	at 2 V (Note 1)
t_3	CLK Low Time	11		ns	Figure 1	at 0.8 V (Note 1)
t_4	CLK Fall Time		3	ns	Figure 1	(2.0 V–0.8 V) (Note 1)
t_5	CLK Rise Time		3	ns	Figure 1	(0.8 V–2.0 V) (Note 1)
t_6	A31–A2, PWT, PCD, $\overline{BE3}$–$\overline{BE0}$, M/$\overline{IO}$, D/$\overline{C}$, W/$\overline{R}$, $\overline{ADS}$, $\overline{LOCK}$, $\overline{FERR}$, BREQ, HLDA Valid Delay	3	14	ns	Figure 5	
t_7	A31–A2, PWT, PCD, $\overline{BE3}$–$\overline{BE0}$, M/$\overline{IO}$, D/$\overline{C}$, W/$\overline{R}$, $\overline{ADS}$, $\overline{LOCK}$, $\overline{FERR}$, BREQ Float Delay		20	ns	Figure 6	Note 1
t_8	$\overline{PCHK}$ Valid Delay	3	14	ns	Figure 5	Note 3
t_{8a}	$\overline{BLAST}$, $\overline{PLOCK}$ Valid Delay	3	14	ns	Figure 5	Note 3
t_9	$\overline{BLAST}$, $\overline{PLOCK}$ Float Delay		20	ns	Figure 6	Note 1
t_{10}	D31–D0, DP3–DP0 Write Data Valid Delay	3	14	ns	Figure 5	Note 3
t_{11}	D31–D0, DP3–DP0 Write Data Float Delay		20	ns	Figure 6	Note 1
t_{12}	$\overline{EADS}$ Setup Time	5		ns	Figure 2	
t_{13}	$\overline{EADS}$ Hold Time	3		ns	Figure 2	
t_{14}	$\overline{KEN}$, $\overline{BS16}$, $\overline{BS8}$ Setup Time	5		ns	Figure 2	
t_{15}	$\overline{KEN}$, $\overline{BS16}$, $\overline{BS8}$ Hold Time	3		ns	Figure 2	
t_{16}	$\overline{RDY}$, $\overline{BRDY}$ Setup Time	5		ns	Figure 3	
t_{17}	$\overline{RDY}$, $\overline{BRDY}$ Hold Time	3		ns	Figure 3	
t_{18}	$\overline{HOLD}$, $\overline{AHOLD}$ Setup Time	6		ns	Figure 2	
t_{18a}	$\overline{BOFF}$ Setup Time	7		ns	Figure 2	
t_{19}	HOLD, AHOLD, $\overline{BOFF}$ Hold Time	3		ns	Figure 2	
t_{20}	RESET, $\overline{FLUSH}$, $\overline{A20M}$, NMI, INTR, $\overline{IGNNE}$ Setup Time	5		ns	Figure 2	Note 4
t_{21}	RESET, $\overline{FLUSH}$, $\overline{A20M}$, NMI, INTR, $\overline{IGNNE}$ Hold Time	3		ns	Figure 2	Note 4
t_{22}	D31–D0, DP3–DP0, A31–A4 Read Data Setup Time	5		ns	Figure 2 Figure 3	
t_{23}	D31–D0, DP3–DP0, A31–A4 Read Data Hold Time	3		ns	Figure 2 Figure 3	

Notes:

1. *Not 100% tested. Guaranteed by design characterization.*
2. *Specifications assume C_L = 50 pF. I/O Buffer model must be used to determine delays due to loading (trace and component). First Order I/O buffer models for the Am486 CPU are available.*
3. *The minimum Am486DX2 CPU output valid delays are hold times provided to external circuitry.*
4. *A reset pulse width of 15 CLK cycles is required for warm resets. Power up resets require RESET to be asserted for at least 1 ms after V_{CC} and CLK are stable.*

66-MHz Am486 Microprocessor AC Characteristics for Boundary Scan Test Signals at 25 MHz

V_{CC} = 5 V ±5%; T_{CASE} = 0°C to +85°C; C_L = 0 pF unless otherwise specified

Symbol	Parameter	Preliminary		Unit	Figure	Notes
		Min	Max			
t_{24}	TCK Frequency		25	MHz		1X Clock
t_{25}	TCK Period	40		ns		Note 2
t_{26}	TCK High Time	10		ns		@ 2.0 V
t_{27}	TCK Low Time	10		ns		@ 0.8 V
t_{28}	TCK Rise Time		4	ns		Note 1
t_{29}	TCK Fall Time		4	ns		Note 1
t_{30}	TDI, TMS Setup Time	8		ns	Figure 7	Note 3
t_{31}	TDI, TMS Hold Time	7		ns	Figure 7	Note 3
t_{32}	TDO Valid Delay	3	25	ns	Figure 7	Note 3
t_{33}	TDO Float Delay		36	ns	Figure 7	Note 3
t_{34}	All Outputs (Non-Test) Valid Delay	3	25	ns	Figure 7	Note 3
t_{35}	All Outputs (Non-Test) Float Delay		36	ns	Figure 7	Note 3
t_{36}	All Inputs (Non-Test) Setup Time	8		ns	Figure 7	Note 3
t_{37}	All Inputs (Non-Test) Hold Time	7		ns	Figure 7	Note 3

Notes:

1. *Rise/Fall times are measured between 0.8 V and 2.0 V. Rise/Fall times can be relaxed by 1 ns per 10-ns increase in TCK period.*
2. *TCK period ≥ CLK period.*
3. *Parameter measured from TCK.*
4. *Boundary Scan AC Specifications in the above table are target values. They have not been characterized. Therefore, they are subject to change.*

Package Thermal Specifications

The Am486DX2-66 microprocessor is specified for operation when T_{case} (the case temperature) is within the range of 0°C to +85°C. T_{case} can be measured in any environment to determine whether the Am486DX2-66 microprocessor is within specified operating range. The case temperature should be measured at the center of the top surface opposite the pins.

The ambient temperature (T_A) is guaranteed as long as T_{CASE} is not violated. The ambient temperature can be calculated from θ_{JC} and θ_{JA} and from the following equations:

$$T_J = T_C + P \cdot \theta_{JC}$$

$$T_A = T_J - P \cdot \theta_{JA}$$

$$T_{CASE} = T_A + P \cdot [\theta_{JA} - \theta_{JC}]$$

where:

T_J, T_A, T_{CASE} = Junction, Ambient, and Case Temperature.

θ_{JC}, θ_{JA} = Junction-to-Case and Junction-to-Ambient Thermal Resistance, respectively.

P = Maximum Power Consumption

The values for θ_{JA} and θ_{JC} are given in Table 1 for the 1.75 sq. in., 168-pin, ceramic PGA.

Table 2 shows the T_A allowable (without exceeding T_{case}) at various airflows and operating frequencies (CLOCK). Note that T_A is greatly improved by attaching "fins" or a "heat sink" to the package. Conventional heat sink dimensions are shown in Figure 1. P (the maximum power consumption) is calculated by using the maximum I_{CC} at 5 V as tabulated in the *DC Characteristics*.

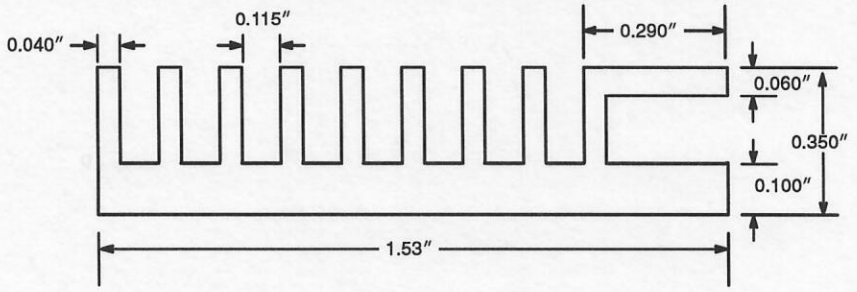
Table 1. Thermal Resistance (°C/W) θ_{JC} and θ_{JA} for the 66-MHz Am486DX2 CPU

	θ_{JA} vs. Airflow–ft/min. (m/sec)						
	θ_{JC}	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
Without Heat Sink	1.5	16.5	14.0	12.0	10.5	9.5	9.0
With Heat Sink*	2.0	12.0	7.0	5.0	4.0	3.5	3.25
With Heat Sink and Fan	2.0	5.0	4.6	4.2	3.8	3.5	3.25

**0.350" high unidirectional heat sink (Al alloy 6063, 40 mil fin width, 155 mil center-to-center fin spacing).*

Table 2. Maximum T_A at Various Airflows in °C

	Airflow–ft/min. (m/sec)						
	CLOCK (MHz)	0 (0)	200 (1.01)	400 (2.03)	500 (3.04)	800 (4.06)	1000 (5.07)
T_A with Heat Sink	66	25	55	67	73	76	77.5
T_A without Heat Sink	66	–	10	22	31	37	40
T_A with Heat Sink and Fan	66	67	69	71.5	74	76	77.5



17852A–113

Figure 1. Heat Sink Dimensions