Outline

• 0.25um Process Description
• Chip Overview
• New Features
• Process Migration Challenges
• Design Methodology Optimizations
• Conclusion
# 0.25um Process Dimensions

- **Gate Oxide Thickness**: 4.8nm
- **Polysilicon Width/Space**: 0.25/0.375um
- **Local Interconnect Pitch**: 0.625um
- **Metal 1 pitch**: 0.875um
- **Metal 2 pitch**: 0.875um
- **Metal 3 pitch**: 0.875um
- **Metal 4 pitch**: 1.125um
- **Metal 5 pitch**: 3.0um
Cross Section of .25um Process

Metal Five (aluminum)
VIA (tungsten)
Metal Four (aluminum)
Metal Three (aluminum)
Metal Two (aluminum)
Metal One (aluminum)
Local Intercon. (tungsten)
AMD-K6 3D™ Overview

- 350MHz frequency of operation
- Small 80 mm² die size
- Less than 50% power of 0.35um AMD-K6
- Multimedia performance enhancements
- Frontside 100MHz bus and L2 cache support
- High performance Enhanced Socket 7 interface
Cycle Time versus Voltage Schmoo

360MHz @ 2.2V
Super7: Socket 7 Enhancement Initiative

- Key Performance Enhancements
  - 2X AGP in ‘97
  - Higher local bus frequency - 100 MHz
  - Support for 100 MHz frontside (Level-2) cache
  - Maintains socket 7 compatibility and cost advantages

- At Leading Edge of all System Features
  - Standard: USB, SDRAM, UDMA, ACPI
  - Enhanced: 2X AGP, PC 98, 100MHz bus, 100MHz SDRAM, 1394, etc

- 3rd Party System Logic
Super7 System
with the AMD-K6 3D Processor

AMD-K6 3D

Frontside Level 2 Cache

100MHz Socket7 Interface

Main Memory

100MHz

NorthBridge

AGP

Video Graphics

PCI

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100MHz bus interface design

- Clock uncertainties are a larger fraction of the cycle time and do not scale with frequency.
- Reduce input setup times and output valid max delays
  - Done by absorbing clock uncertainties into the core
- Improve the cycle time of "loop-back" paths.
  - Done by removing the uncertainties in a clock domain crossing.
100 MHz Loop-back Logic Paths

Fig a
Old Scheme

Fig b
Waveforms

Fig c
New Scheme
AMD-3D Technology Motivations

- X87 is the single largest bottleneck today
- MMX and graphics accelerator boards only operate on integer data.
- AMD-3D accelerates the floating point intensive stages of the graphics pipeline.
- Realistic physical modeling is also becoming a necessity.
AMD-3D Technology Definition

- SIMD Floating Point Instructions
  - Supports IEEE single precision data storage format
  - Two 32-bit FP values per 64-bit reg/mem operand
  - Uses MMX registers
- 21 New Instructions
- Streamlined for High Performance
  - Saturating arithmetic
  - No exceptions
  - Limited rounding modes
  - No switching overhead between MMX and AMD-3D
- No Core OS Support Required
AMD-3D Technology: Market Support

- Enthusiastic Support from Major ISV's
- Full Software Development Support
  - Full Microsoft Support
    - Assembly language - native support
    - Fully optimized API and libraries at introduction: DirectX (Direct3D & DirectSound) and OpenGL
  - Profiler and optimizer tools
- Licensed to other x86 processor vendors
- Dedicated AMD Development Support Group
Coupled AMD-3D, MMX Execution Unit

• Superscalar pipelined instruction issue
• All instruction dependencies resolved internally
• All floating point AMD-3D instructions
  • Similar encoding to MMX instructions
  • Have a latency of 2 cycles and are fully pipelined
• 4 floating point operations per cycle throughput
  • 2 ops/instruction X 2 instructions/cycle
• CPI improvement by over 20% on MMX benchmarks due to Superscalar and Pipelined MMX execution
Multimedia Unit Resources

Register X Execution Pipeline

Shared Resources

FP Add
Recip / RecipSqrt

MMX+FP Multiplier

MMX Shifter

Register Y Execution Pipeline

MMX ALU

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Memory Subsystem Enhancements

- More aggressive pipelining of data reads and writes on the system bus.
- Speculative data cache fills.
- Completion of stores while a data cache fill is in progress.
- 2% to 10% CPI improvement on various benchmarks.
Input/Output Circuit Design

- Core voltage of 2.5V max, but 3.3V I/O
- Could not include transistors with thicker oxides in process due to fab throughput constraints.
- Gate oxide protection scheme
Protected Output Driver

Vddio

Vcore

Level-Shifter

Buffer

Output Driver

VREF1

VREF2

Dout

PAD

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I/O Reference Voltage Generation

Bandgap Voltage Reference

R3 = R4 = R5 = R6

VREF2 = 1.8V

VREF1 = Vddio - 1.8V

Vddio
Power-On Reset Circuit

- Some chip state is required to not change during chip reset ==> This state can only be initialized during power-up. (eg., JTAG)
- Power-On Reset is released when all chip inputs and supplies are stable, regardless of supply sequence and ramp rates.
- The circuit functions correctly over a wide range of operating conditions.
Power-On Reset Circuit

I/O replica
transfer a “0”

I/O replica
transfer a “1”

VDD ramp sensor

Vddio

Vdd

Vtn+Vtp

delay

Reset
VDD Ramp Sensor

Vdd

R1

Vdd

vt

sense

R2

vdd_trip
Power-On Reset Simulation Waveforms

- I/O supply
- Core supply
- Ground
- VDDIO
- VDD core
- Reset

Time

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Circuit Verification

• Guarantee robust operation across all process variations by simulating custom circuits at 10 process corners
• Electromigration analysis for 10+ year reliable lifespan
• Less than 2% frequency degradation over lifetime due to Hot Carrier Injection
Hold-Time Analysis

- Analysis maximizes skew, minimizes data delays
  - Extracted R & C on clock network
  - Worst possible cross-die device mismatches
  - Fastest possible transistors for signal paths
  - Reduced R & C on signal nets
- Uses point-to-point clock skew from simulation
- Automatically:
  - Replaces fast registers with slower ones
  - Re-sizes existing delay cells
  - Adds delay cells & shares when possible
Full Chip Clock Skew
Datapath Construction Methodology

- New interactive, graphical, in-house, cell placement tool
- New automated datapath router (Vendor Tool)
- Allowed exploration of more “what-if” scenarios
- More optimal for schedule, timing, and area.
Conclusion

- The AMD-K6 3D processor is a follow-on to the AMD-K6 MMX Enhanced processor
- Manufactured on AMD’s 0.25um process
- Supports AMD’s Super 7 initiative with its 100MHz bus interface
- Introduces AMD-3D technology
- Transistor Density
  - 11 Million transistors on an 80 mm² die!