Chapter 5
Tables

Table 5.1 RAMBUS CHANNEL PINS AND SIGNAL TYPES

Pin	Signal Type and Notes
BusData (eight-nine bits)	"active" RSL (low-voltage Rambus Signaling Logic); data
BusEnable	"active" RSL; enable, reset
BusCtrl	"active" RSL; packet framing, opcode xfer, ack
ClkToMaster	"active" RSL; sync for data from slaves
ClkFromMaster	"active" RSL; sync for data from master
SIn and SOut	"active" TTL; address configuration and refresh
Vref	Voltage reference for all RSL signals
Gnd, Vdd	power
GndA, VddA	"analog" power for PLLs
isolation (two pins)	—
reserved (one pin)	—