6x86L PROCESSOR

Sixth-Generation Superscalar
Superpipelined x86-Compatible CPU

6x86L PROCESSOR ADDENDUM

♦ Low Voltage Operation

- 2.8 volt core operation
- 3.3 volt I/O interface
- Greater than 25% power reduction (compared to the 6x86)
- 296 SPGA, Socket 7 compatible
- 100, 110, 120, 133, and 150 MHz core operation

♦ Sixth-Generation Superscalar Superpipelined Architecture

- Dual 7-stage integer pipelines
- High performance 80-bit FPU with 64-bit interface
- 16-KByte unified write-back L1 cache

♦ X86 Instruction Set Compatible

- Runs Windows 95, Windows 3.x, Windows NT, DOS, UNIX, OS/2, Solaris, and other operating systems
- Optimized to run both 16-bit and 32-bit software applications

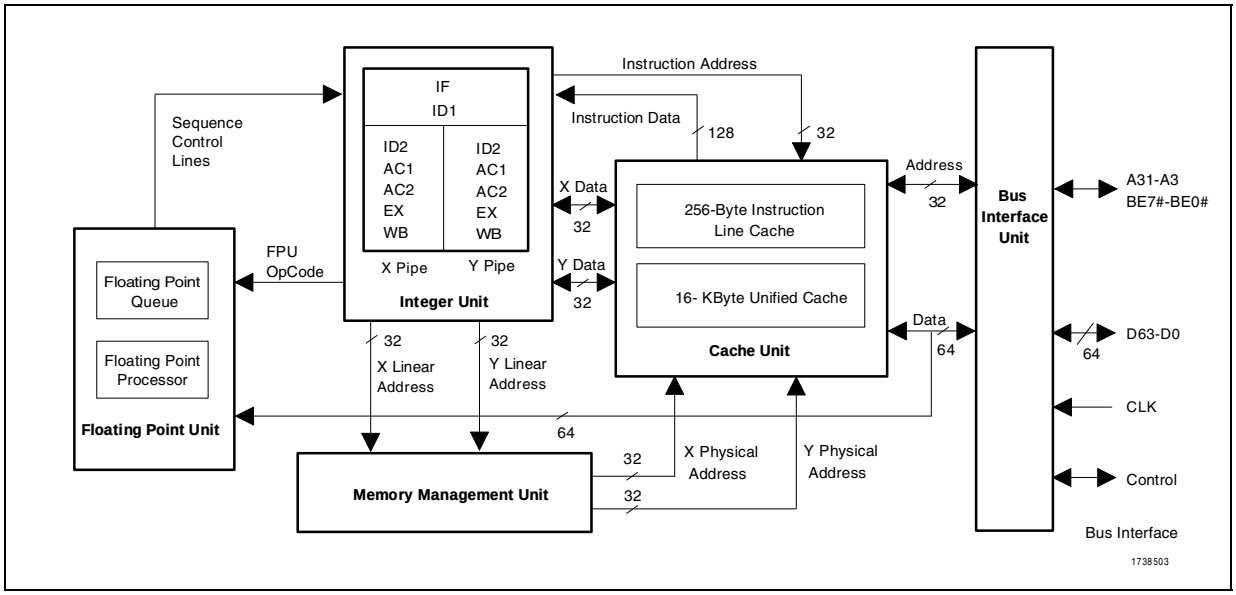
♦ Best Performance Through Superior Architecture

- Intelligent instruction dispatch
- Register renaming, out-of-order completion
- Data dependency removal, multi-branch prediction
- Speculative execution

The 6x86L CPUs use two power supplies; one supply is for the core, and the other is for the I/O interface. The 6x86L logically functions the same way as previous versions of the 6x86.

The Cyrix 6x86L™ processor is a superscalar, superpipelined sixth-generation CPU optimized to run both 16-bit and 32-bit software applications. The 6x86 processor is fully compatible with the x86 instruction set and delivers industry-leading performance running Windows® 95, Windows, Windows NT, OS/2,® DOS Solaris, UNIX® and other operating systems.

The 6x86L processor achieves top performance through the use of two optimized superpipelined integer units and an on-chip floating point unit. The superpipelined architecture reduces timing constraints and increases frequency scalability to 150 MHz and beyond. Additionally, the integer and floating point units are optimized for maximum instruction throughput by using advanced architectural techniques including register renaming, out-of-order completion, data dependency removal, branch prediction and speculative execution.



August 28, 1996 4:37 pm
Revision 0.99N
c:\dataoem\m11\m11.fm
Rev N: Changed output valid delay 2 items, AC3 & AC5->NC
Rev. M: Changed parameter and units Table 2-4 p7
Rev L: Changed page 13, removed line T26
Rev K: Added Device Identification
Rev J: Changed low voltage bullets, deleted table 1-1 & T26
Rev I: Changed Vcc2 to 2.97 v page 5; fixed orphan page 3
Rev H: Updated bullets, 6x86->6x86L, Icc, Vcc

1.0 OVERVIEW

This addendum to the *6x86 Processor Data Book* documents describes the 6x86L product family of Cyrix 6x86 CPUs.

The 6x86L requires two power supply voltages, one core voltage of typically 2.8 volts and a I/O voltage of 3.3 volts. Refer to Table 2-2 (Page 5) for details. In addition, the 6x86L CPU adds debug capabilities and a new instruction. Some minor signal pin changes also have been made that do not affect standard systems operation.

1.1 New Instruction

The CMPXCHG8B *(Compare and Exchange 8 Bytes)* instruction has been added for compatibility with next generation software. This instruction compares the 64-bit value in the EDX:EAX register with the r/m qword within 13 clock counts. If equal, ZF is set and ECX:EBX is loaded into the r/m qword. If not equal, ZF is cleared and the qword is loaded into EDX:EAX. This instruction has the following opcode:

0F C7 [mod 001 r/m]

1.2 Device Identification

The 6x86 and 6x86L devices are identified by device identification registers DIR0 and DIR1 as shown in Table 1-1.

.

Table 1-1. Device Identification

DEVICE	DIR0	DIR1
6x86	31h	0xh or 1xh
6x86L		2xh

where x is any hexadecimal number.

1.3 New Register

The CR4 register has been added to include the DE (Debug Extension) bit 3 in CR4. The DE bit is used to modify the meaning of the R/W bits in the debug control register (DR7). If DE is set, and the particular R/Wn bits are set to 10, an I/0 read or write will trigger one of four breakpoints. If DE is not set, an I/O read or write will not trigger a breakpoint in any case.

2.0 ELECTRICAL SPECIFICATIONS

2.1 Power and Ground Connections

The 6x86L CPU contains 296 pins with 25 pins connected to V_{CC2} (2.8 volts), 28 pins connected to V_{CC3} (3.3 volts), and 53 pins connected to V_{SS} (ground).

2.2 Signal Pin Changes

The signals DHOLD, BHOLD, LBA# and QDUMP# are not supported by this CPU revision. These signals were used to support non-industry standard systems and their omission does not effect standard systems operation.

The Vcc2DET output pin is connected within the 6x86L CPU to V_{SS} to indicate to the system that a dual voltage power supply is required.

2.2.1 Unused Input Pins

All inputs not used by the system designer and not listed in Table 4-1 in the *6x86 Processor Data Book* should be connected either to ground or to V_{CC3} (3.3 V). Connect active-high inputs to ground through a pull-down resistor (20 kΩ ± 10%) and active-low inputs to V_{CC3} (3.3 V) through a pull-up resistor (20 kΩ ± 10%) to prevent possible spurious operation.

2.2.2 NC and Reserved Pins

Pins designated NC (no connect) are not internally connected. Pins designated "RESV or Reserved" are special pins for use by Cyrix and should be left disconnected. Connecting a reserved pin to a pull-up resistor, pull-down resistor, or an active signal could cause unexpected results and possible circuit malfunctions.

2.3 Operating Voltages

The 6x86L CPU operates using two power supply voltages—one for the I/O (3.3 V) and one for the core (2.8 V).

The electrical specifications presented in this addendum augment and replace the electrical specifications presented in the 6x86 Data Book and, if applicable, reference the same notes.

2.4 Absolute Maximum Ratings

The following table lists absolute maximum ratings for the 6x86L processors. Stresses beyond those listed under Table 2-1 limits may cause permanent damage to the device. These are stress ratings only and do not imply that operation under any conditions other than those listed under "Recommended Operating Conditions" Table 2-2 (Page 5) is possible. Exposure to conditions beyond Table 2-1 may (1) reduce device reliability and (2) result in premature failure even when there is no immediately apparent sign of failure. Prolonged exposure to conditions at or near the absolute maximum ratings may also result in reduced useful life and reliability.

Table 2-1. Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNITS	NOTES
Operating Case Temperature	-65	110	°C	Power Applied
Storage Temperature	-65	150	°C	
Supply Voltage, V_{CC3}	-0.5	4.0	V	
Supply Voltage, V_{CC2}	-0.5	3.3	V	
Voltage On Any Pin	-0.5	V_{CC3} + 0.5	V	
Input Clamp Current, I_{IK}		10	mA	Power Applied
Output Clamp Current, I_{OK}		25	mA	Power Applied

2.5 Recommended Operating Conditions

Table 2-2 presents the recommended operating conditions for the 6x86L CPU device.

Table 2-2. Recommended Operating Conditions

PARAMETER	MIN	MAX	UNITS	NOTES
T_C Operating Case Temperature	0	70	°C	Power Applied
V_{CC3} Supply Voltage (3.3 V)	3.15	3.45	V	
V_{CC2} Supply Voltage (2.8 V)	2.63	2.97	V	
V_{IH} High-Level Input Voltage (except CLK)	2.00	3.55	V	
V_{IH} CLK High-Level Input Voltage	2.0	5.5	V	
V_{IL} Low-Level Input Voltage	-0.3	0.8	V	
I_{OH} High-Level Output Current		-1.0	mA	$V_O=V_{OH(MIN)}$
I_{OL} Low-Level Output Current		5.0	mA	$V_O=V_{OL(MAX)}$

2.6 DC Characteristics

Table 2-3. DC Characteristics (at Recommended Operating Conditions) 1of 2

PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{OL} Low-Level Output Voltage			0.4	V	I_{OL} = 5 mA
V_{OH} High-Level Output Voltage	2.4			V	I_{OH} = -1 mA
I_I Input Leakage Current For all pins (except those listed in Table 4-1 of the Cyrix 6x86 Microprocessor Data Book).			±15	µA	$0 < V_{IN} < V_{CC3}$ Note 1
I_{IH} Input Leakage Current For all pins with internal pull-downs.			200	µA	V_{IH} = 2.4 V Note 1
I_{IL} Input Leakage Current For all pins with internal pull-ups.			-400	µA	V_{IL} = 0.45 V Note 1
C_{IN} Input Capacitance			15	pF	f = 1 MHz*
C_{OUT} Output Capacitance			20	pF	f = 1 MHz*
C_{IO} I/O Capacitance			25	pF	f = 1 MHz*
C_{CLK} CLK Capacitance			15	pF	f = 1 MHz*

*Note: Not 100% tested.

Table 2-4. DC Characteristics (at Recommended Operating Conditions) 2 of 2

PARAMETER	CORE		I/O		UNITS	NOTES
	TYP	MAX	TYP	MAX		
I_{CC} Active I_{CC}						Notes 1, 2
P120+ (100 MHz)	3900	4700	65	75	mA	
P133+ (110 MHz)	4100	5000	70	80		
P150+ (120 MHz)	4400	5300	72	85		
P166+ (133 MHz)	4700	5600	77	90		
P200+ (150 MHz)	5000	6000	84	100		
I_{CCSM} Suspend Mode I_{CC}						Notes 1, 2, 3
P120+ (100 MHz)	60	75	6	8	mA	
P133+ (110 MHz)	65	80	6	8		
P150+ (120 MHz)	70	85	6	8		
P166+ (133 MHz)	75	90	6	8		
P200+ (150 MHz)	85	100	6	8		
I_{CCSS} Standby I_{CC}						
0 MHz (Suspended/CLK Stopped)	55	70	5	7	mA	Notes 2, 4

Notes:
1. Frequency (MHz) ratings refer to the internal clock frequency.
2. Typical values are measured at 2.8 V.
3. All inputs at 0.4 or V_{CC3} - 0.4 (CMOS levels). All inputs held static except clock and all outputs unloaded (static I_{OUT} = 0 mA).
4. All inputs at 0.4 or V_{CC3} - 0.4 (CMOS levels). All inputs held static and all outputs unloaded (static I_{OUT} = 0 mA).

2.7 AC Characteristics

Tables 2-5 through 2-10 (Pages 9 through 13) list the AC characteristics including output delays, input setup requirements, input hold requirements and output float delays. These measurements are based on the measurement points identified in Figure 2-1 (Page 9) and Figure 2-2 (Page 10). The rising clock edge reference level V_{REF} and other reference levels are shown in Table 2-5. Input or output signals must cross these levels during testing.

Figure 2-1 shows output delay (A and B) and input setup and hold times (C and D). Input setup and hold times (C and D) are specified minimums, defining the smallest acceptable sampling window a synchronous input signal must be stable for correct operation.

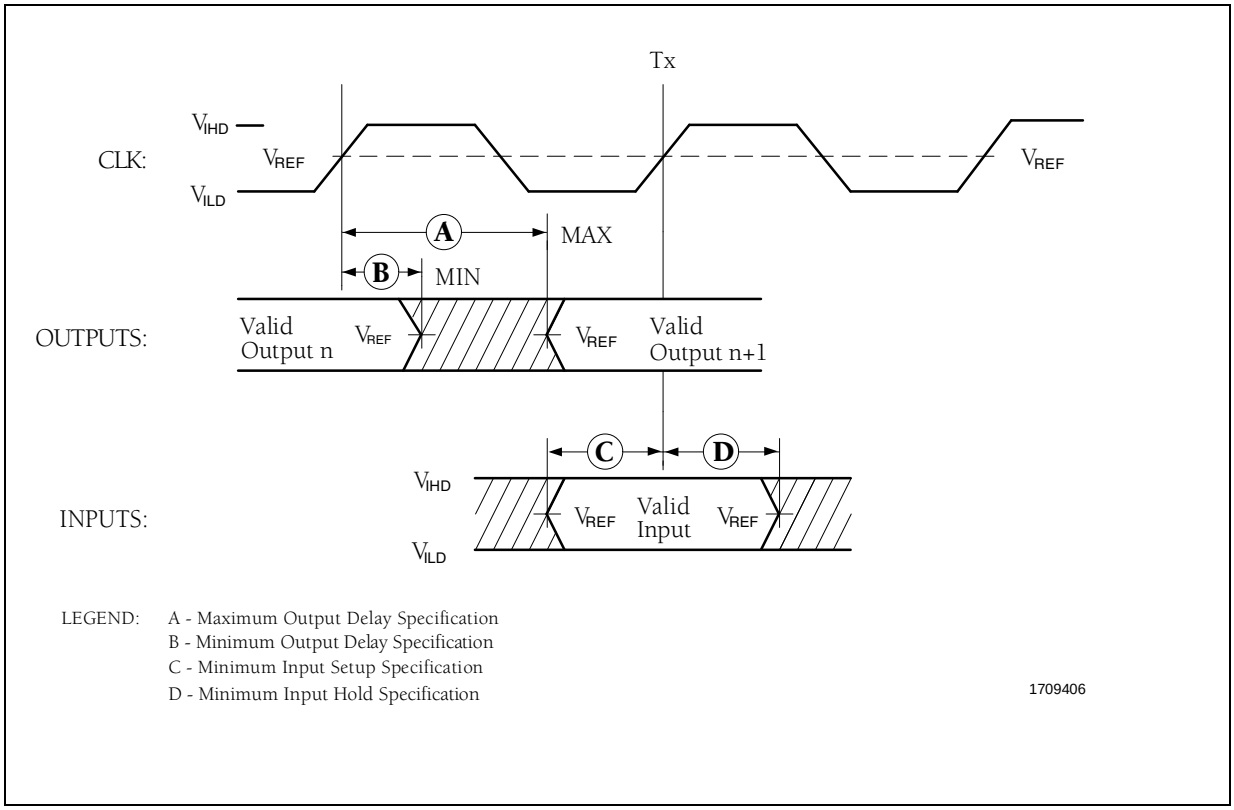


Figure 2-1. Drive Level and Measurement Points for Switching Characteristics

Table 2-5. Drive Level and Measurement Points for Switching Characteristics

SYMBOL	VOLTAGE (Volts)
V_{REF}	1.5
V_{IHD}	2.3
V_{ILD}	0

Note: Refer to Figure 2-1.

Table 2-6. Clock Specifications

T_{CASE} = 0°C to 70°C, See Figure 2-2

SYMBOL	PARAMETER	50-MHz BUS		55-MHz BUS		60-MHz BUS		66-MHz BUS		75-MHz BUS		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	CLK Frequency		50		55		60		66.6		75	MHz
T1	CLK Period	20		18		16.67	33.33	15.0	30.0	13.3		ns
T2	CLK Period Stability		± 250		±250		±250		±250		± 250	ps
T3	CLK High Time	7		4.0		4.0		4.0		4.0		ns
T4	CLK Low Time	7		4.0		4.0		4.0		4.0		ns
T5	CLK Fall Time	0.15	2	0.15	1.5	0.15	1.5	0.15	1.5	0.15	1.5	ns
T6	CLK Rise Time	0.15	2	0.15	1.5	0.15	1.5	0.15	1.5	0.15	1.5	ns

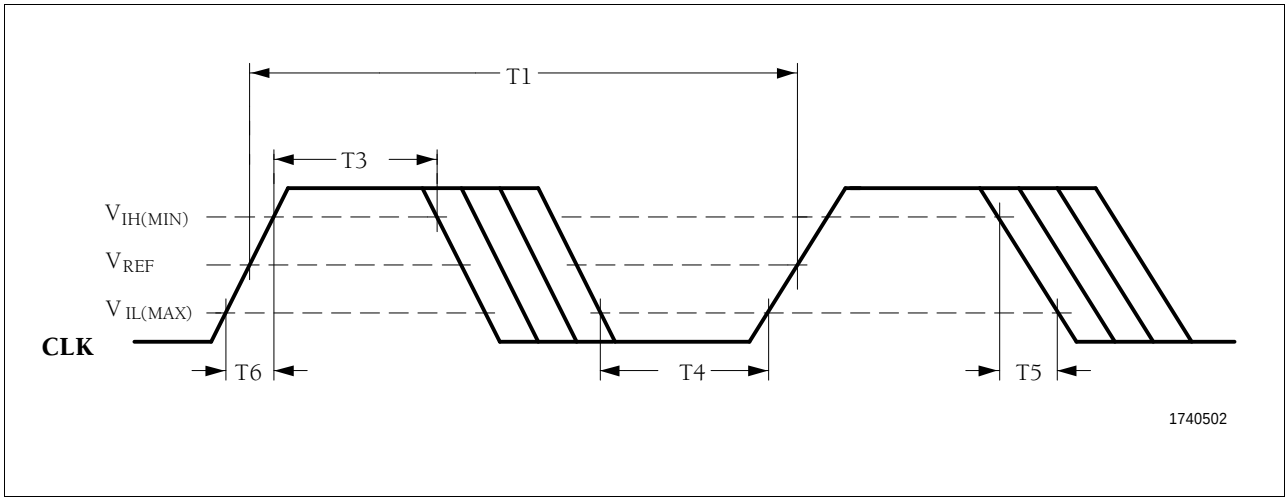


Figure 2-2. CLK Timing and Measurement Points

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Table 2-7. Output Valid Delays

C_L = 50 pF, T_{case} = 0°C to 70°C, See Figure 2-3

	PARAMETER	50-MHz BUS		55-MHz BUS		60-MHz BUS		66-MHz BUS		75-MHz BUS		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
T7a	A31-A3, BE7#-BE0#, CACHE#, D/C#, LOCK#, PCD, PWT, SCYC, SMIACT#, W/R#	1.0	12	1.0	7.0	1.0	7.0	1.0	7.0	1.0	7.0	ns
T7b	ADS#, M/IO#	1.0	12	1.0	7.0	1.0	7.0	1.0	7.0	1.0	6.0	ns
T8	ADSC#	1.0	12	1.0	7.0	1.0	7.0	1.0	7.0	1.0	7.0	ns
T9	AP	1.0	12	1.0	8.5	1.0	8.5	1.0	8.5	1.0	8.5	ns
T10	APCHK#, PCHK#, FERR#	1.0	14	1.0	8.3	1.0	7.0	1.0	7.0	1.0	7.0	ns
T11	D63-D0, DP7-DP0 (Write)	1.3	12	1.3	8.5	1.3	7.5	1.3	7.5	1.0	7.5	ns
T12a	HIT#	1.0	12	1.0	8.0	1.0	8.0	1.0	8.0	1.0	8.0	ns
T12b	HITM#	1.1	12	1.1	6.0	1.1	6.0	1.1	6.0	1.1	6.0	ns
T13	BREQ, HLDA	1.0	12	1.0	8.0	1.0	8.0	1.0	8.0	1.0	8.0	ns
T14	SUSPA#	1.0	14	1.0	8.0	1.0	8.0	1.0	8.0	1.0	8.0	ns

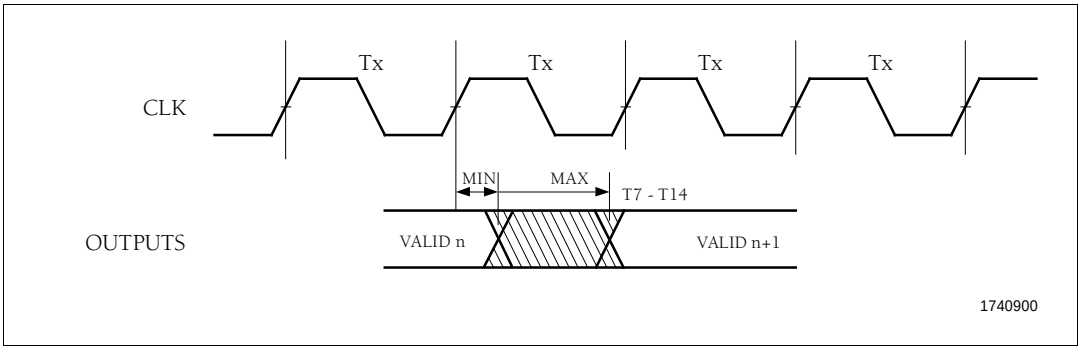

Figure 2-3. Output Valid Delay Timing

Table 2-8. Output Float Delays

C_L = 50 pF, T_{case} = 0°C to 70°C, See Figure 2-5

	PARAMETER	50-MHz BUS		55-MHz BUS		60-MHz BUS		66-MHz BUS		75-MHz BUS		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
T15	A31-A3, ADS#, BE7#-BE0#, BREQ, CACHE#, D/C#, LOCK#, M/IO#, PCD, PWT, SCYC, SMI-ACT#, W/R#		16		10.0		10.0		10.0		10	ns
T16	AP		16		10.0		10.0		10.0		10	ns
T17	D63-D0, DP7-DP0 (Write)		16		10.0		10.0		10.0		10	ns

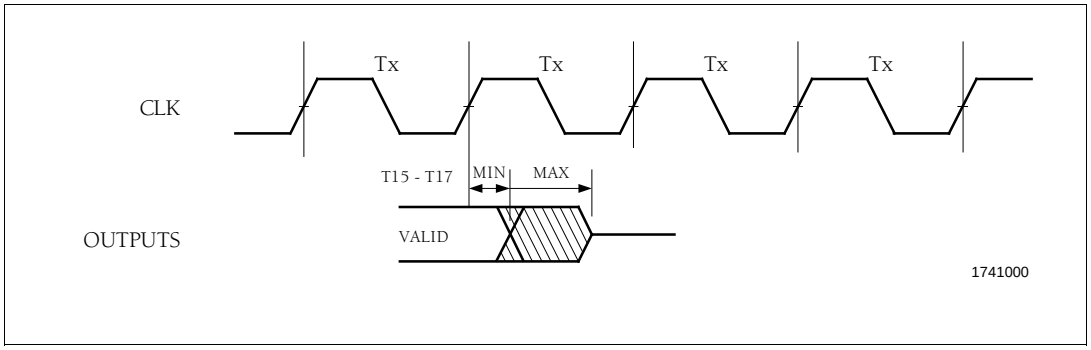

Figure 2-4. Output Float Delay Timing

Table 2-9. Input Setup Times

T_{case} = 0°C to 70°C, See Figure 2-5

	PARAMETER	50-MHz BUS	55-MHz BUS	60-MHz BUS	66-MHz BUS	75-MHz BUS	UNITS
		MIN	MIN	MIN	MIN	MIN	
T18	A20M#, FLUSH#, IGNNE#, SUSP#	5.0	5.0	5.0	5.0	3.3	ns
T19	AHOLD, BOFF#, HOLD	5.0	5.0	5.0	5.0	3.3	ns
T20	BRDY#	5.0	5.0	5.0	5.0	3.3	ns
T21	BRDYC#	5.0	5.0	5.0	5.0	3.3	ns
T22a	A31-A3, AP, BE7#-BE0#,	5.0	5.0	5.0	5.0	3.3	ns
T22b	AP	5.0	5.0	5.0	5.0	4.0	ns
T22c	D63-D0 (Read), DP7-DP0 (Read)	5.0	3.8	3.0	3.0	3.0	ns
T23	EADS#, INV	5.0	5.0	5.0	5.0	3.3	ns
T24	INTR, NMI, RESET, SMI#, WM_RST	5.0	5.0	5.0	5.0	3.3	ns
T25	EWBE#, KEN#, NA#, WB/WT#	5.0	4.5	4.5	4.5	3.0	ns

Table 2-10. Input Hold Times

T_{case} = 0°C to 70°C, See Figure 2-5

SYMBOL	PARAMETER	50-MHz BUS	55-MHz BUS	60-MHz BUS	66-MHz BUS	75-MHz BUS	UNITS
		MIN	MIN	MIN	MIN	MIN	
T27	A20M#, FLUSH#, IGNNE#, SUSP#	2.0	1.0	1.0	1.0	1.0	ns
T28	AHOLD, BOFF#, HOLD	2.0	1.0	1.0	1.0	1.0	ns
T29	BRDY#	2.0	1.0	1.0	1.0	1.0	ns
T30	BRDYC#	2.0	1.0	1.0	1.0	1.0	ns
T31a	A31-A3, BE7#-BE0#	2.0	1.0	1.0	1.0	1.0	ns
T31b	AP	2.0	1.5	1.5	1.5	1.5	ns
T31c	D63-D0, DP7-DP0 (Read)	2.0	2.0	2.0	2.0	2.0	ns
T32	EADS#, INV	2.0	1.0	1.0	1.0	1.0	ns
T33	INTR, NMI, RESET, SMI#, WM_RST	2.0	1.0	1.0	1.0	1.0	ns
T34	EWBE#, KEN#, NA#, WB/WT#	2.0	1.0	1.0	1.0	1.0	ns

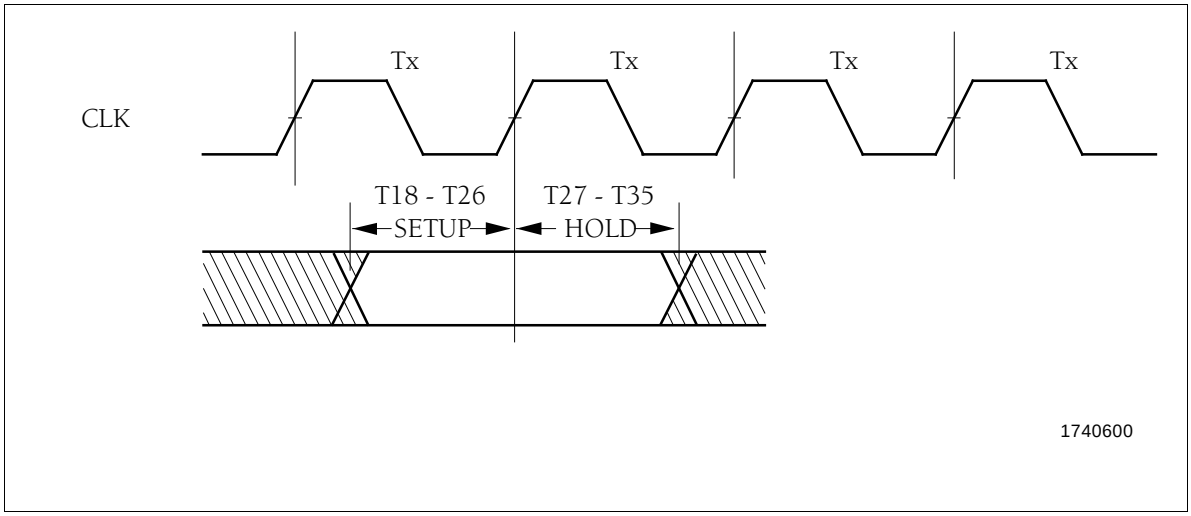

Figure 2-5. Input Setup and Hold Timing

2.8 Pin Differences

The signal description for the pins listed in Table 2-11 have changed from those listed in the *6x86 Processor Data Book*.

Table 2-11. 6x86 vs. 6x86L Pin Differences

PIN NUMBER	6x86	6x86L
A7	Vcc	Vcc2
A9	Vcc	Vcc2
A11	Vcc	Vcc2
A13	Vcc	Vcc2
A15	Vcc	Vcc2
A17	Vcc	Vcc2
G1	Vcc	Vcc2
J1	Vcc	Vcc2
J33	Reserved	NC
L1	Vcc	Vcc2
N1	Vcc	Vcc2
Q1	Vcc	Vcc2
R34	BHOLD	NC
S1	Vcc	Vcc2
S5	LBA#	NC
S35	DHOLD	Reserved
U1	Vcc	Vcc2

PIN NUMBER	6x86	6x86L
W1	Vcc	Vcc2
Y1	Vcc	Vcc2
AA1	Vcc	Vcc2
AA3	Reserved	NC
AC1	Vcc	Vcc2
AC3	Reserved	NC
AE1	Vcc	Vcc2
AG1	Vcc	Vcc2
AL1	NC	Vcc2DET
AL7	QDUMP#	NC
AL19	Reserved	NC
AN9	Vcc	Vcc2
AN11	Vcc	Vcc2
AN13	Vcc	Vcc2
AN15	Vcc	Vcc2
AN17	Vcc	Vcc2
AN19	Vcc	Vcc2

The 6x86 Vcc pins listed in Table 2-12 have been renamed as Vcc3 pins on the 6x86LV.

Table 2-12. Pin Renamed to Vcc3

A19	A29	L37	U33	AC37	AN23
A21	E37	N3	U37	AE37	AN25
A23	G37	Q37	W37	AG37	AN27
A25	J37	S37	Y37	AN21	AN29
A27	L33	T34	AA37		

3.0 MECHANICAL SPECIFICATIONS

3.1 296-Pin SPGA Package

The pin assignments for the 6x86L CPU in a 296-pin SPGA package are shown in Figures 1 and 2. The pins are listed by pin number in Table 3-1 (Page 9) and by signal name in Table 3-2 (Page 10). Dimensions are shown in Figure 3-3 (Page 11) and Table 3-3 (Page 12).

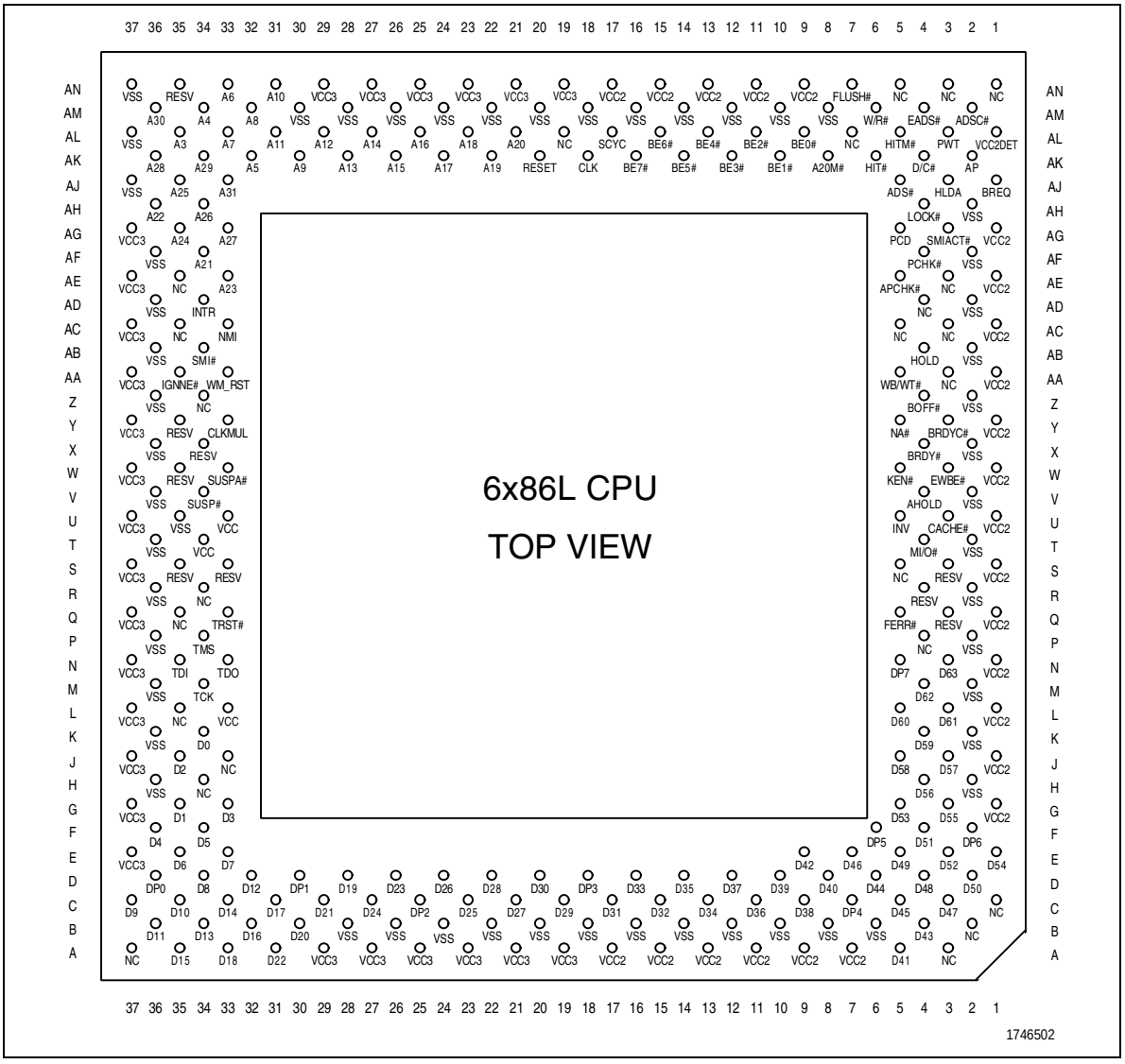

Figure 3-1. 296-Pin SPGA Package Pin Assignments (Top View)

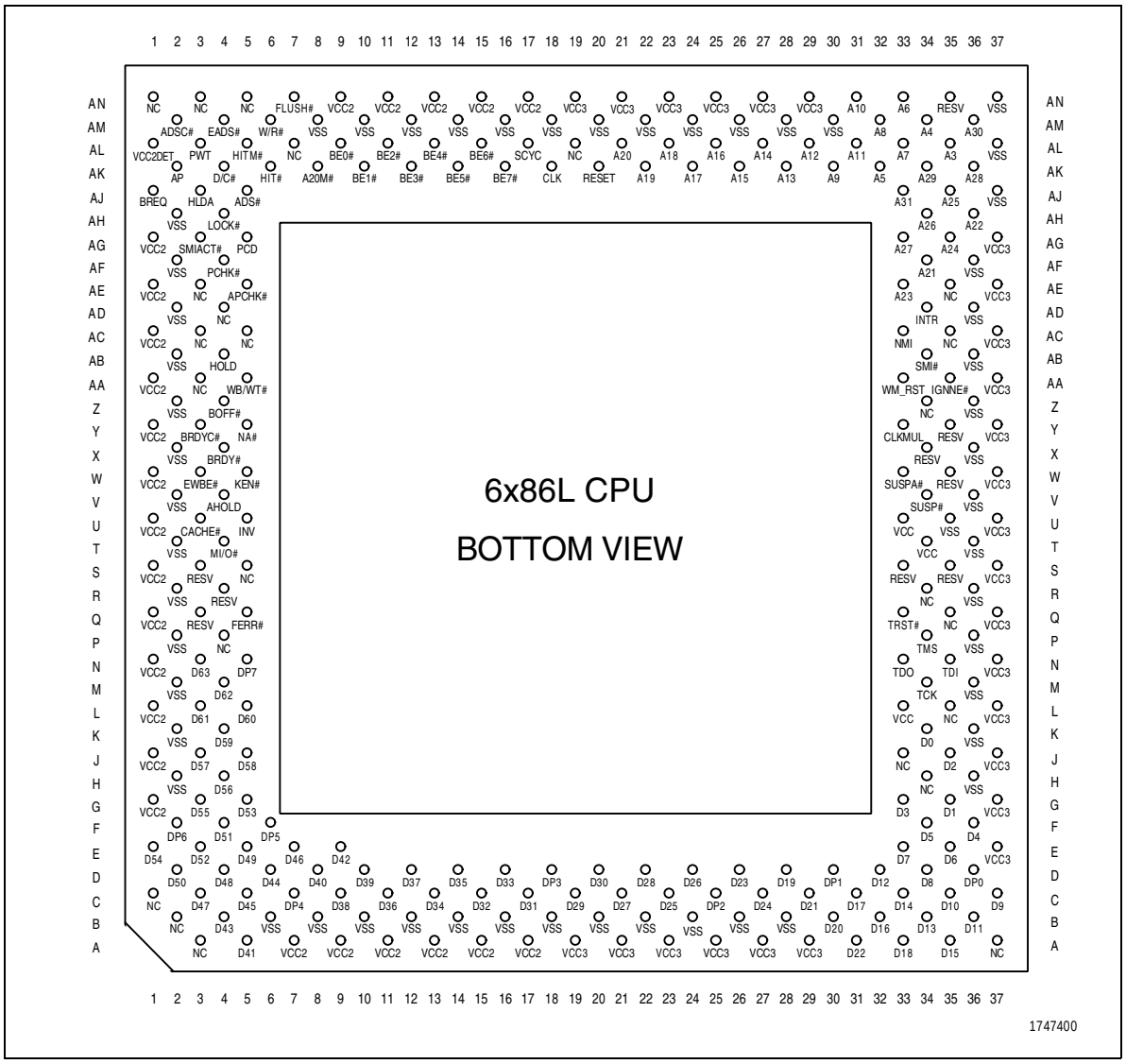

Figure 3-2. 296-Pin SPGA Package Pin Assignments (Bottom View)

Table 3-1. 296-Pin SPGA Package Signal Names Sorted by Pin Number

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A3	NC	C29	D21	J35	D2	U35	Vss	AE35	NC	AL21	A20
A5	D41	C31	D17	J37	Vcc3	U37	Vcc3	AE37	Vcc3	AL23	A18
A7	Vcc2	C33	D14	K2	Vss	V2	Vss	AF2	Vss	AL25	A16
A9	Vcc2	C35	D10	K4	D59	V4	AHOLD	AF4	PCHK#	AL27	A14
A11	Vcc2	C37	D9	K34	D0	V34	SUSP#	AF34	A21	AL29	A12
A13	Vcc2	D2	D50	K36	Vss	V36	Vss	AF36	Vss	AL31	A11
A15	Vcc2	D4	D48	L1	Vcc2	W1	Vcc2	AG1	Vcc2	AL33	A7
A17	Vcc2	D6	D44	L3	D61	W3	EWBE#	AG3	SMIACT#	AL35	A3
A19	Vcc3	D8	D40	L5	D60	W5	KEN#	AG5	PCD	AL37	Vss
A21	Vcc3	D10	D39	L33	Vcc3	W33	SUSPA#	AG33	A27	AM2	ADSC#
A23	Vcc3	D12	D37	L35	NC	W35	Reserved	AG35	A24	AM4	EADS#
A25	Vcc3	D14	D35	L37	Vcc3	W37	Vcc3	AG37	Vcc3	AM6	W/R#
A27	Vcc3	D16	D33	M2	Vss	X2	Vss	AH2	Vss	AM8	Vss
A29	Vcc3	D18	DP3	M4	D62	X4	BRDY#	AH4	LOCK#	AM10	Vss
A31	D22	D20	D30	M34	TCK	X34	Reserved	AH34	A26	AM12	Vss
A33	D18	D22	D28	M36	Vss	X36	Vss	AH36	A22	AM14	Vss
A35	D15	D24	D26	N1	Vcc2	Y1	Vcc2	AJ1	BREQ	AM16	Vss
A37	NC	D26	D23	N3	D63	Y3	BRDYC#	AJ3	HLDA	AM18	Vss
B2	NC	D28	D19	N5	DP7	Y5	NA#	AJ5	ADS#	AM20	Vss
B4	D43	D30	DP1	N33	TDO	Y33	CLKMUL	AJ33	A31	AM22	Vss
B6	Vss	D32	D12	N35	TDI	Y35	Reserved	AJ35	A25	AM24	Vss
B8	Vss	D34	D8	N37	Vcc3	Y37	Vcc3	AJ37	Vss	AM26	Vss
B10	Vss	D36	DP0	P2	Vss	Z2	Vss	AK2	AP	AM28	Vss
B12	Vss	E1	D54	P4	NC	Z4	BOFF#	AK4	D/C#	AM30	Vss
B14	Vss	E3	D52	P34	TMS	Z34	NC	AK6	HIT#	AM32	A8
B16	Vss	E5	D49	P36	Vss	Z36	Vss	AK8	A20M#	AM34	A4
B18	Vss	E7	D46	Q1	Vcc2	AA1	Vcc2	AK10	BE1#	AM36	A30
B20	Vss	E9	D42	Q3	Reserved	AA3	NC	AK12	BE3#	AN1	NC
B22	Vss	E33	D7	Q5	FERR#	AA5	WB/WT#	AK14	BE5#	AN3	NC
B24	Vss	E35	D6	Q33	TRST#	AA33	WM_RST	AK16	BE7#	AN5	NC
B26	Vss	E37	Vcc3	Q35	NC	AA35	IGNNE#	AK18	CLK	AN7	FLUSH#
B28	Vss	F2	DP6	Q37	Vcc3	AA37	Vcc3	AK20	RESET	AN9	Vcc2
B30	D20	F4	D51	R2	Vss	AB2	Vss	AK22	A19	AN11	Vcc2
B32	D16	F6	DP5	R4	Reserved	AB4	HOLD	AK24	A17	AN13	Vcc2
B34	D13	F34	D5	R34	NC	AB34	SMI#	AK26	A15	AN15	Vcc2
B36	D11	F36	D4	R36	Vss	AB36	Vss	AK28	A13	AN17	Vcc2
C1	NC	G1	Vcc2	S1	Vcc2	AC1	Vcc2	AK30	A9	AN19	Vcc2
C3	D47	G3	D55	S3	Reserved	AC3	NC	AK32	A5	AN21	Vcc3
C5	D45	G5	D53	S5	NC	AC5	NC	AK34	A29	AN23	Vcc3
C7	DP4	G33	D3	S33	Reserved	AC33	NMI	AK36	A28	AN25	Vcc3
C9	D38	G35	D1	S35	Reserved	AC35	NC	AL1	Vcc2DET	AN27	Vcc3
C11	D36	G37	Vcc3	S37	Vcc3	AC37	Vcc3	AL3	PWT	AN29	Vcc3
C13	D34	H2	Vss	T2	Vss	AD2	Vss	AL5	HITM#	AN31	A10
C15	D32	H4	D56	T4	MI/O#	AD4	NC	AL7	NC	AN33	A6
C17	D31	H34	NC	T34	Vcc3	AD34	INTR	AL9	BE0#	AN35	Reserved
C19	D29	H36	Vss	T36	Vss	AD36	Vss	AL11	BE2#	AN37	Vss
C21	D27	J1	Vcc2	U1	Vcc2	AE1	Vcc2	AL13	BE4#		
C23	D25	J3	D57	U3	CACHE#	AE3	NC	AL15	BE6#		
C25	DP2	J5	D58	U5	INV	AE5	APCHK#	AL17	SCYC		
C27	D24	J33	NC	U33	Vcc3	AE33	A23	AL19	NC		

Table 3-2. 296-Pin SPGA Package Signal Names Sorted by Signal Names

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
A3	AL35	D/C#	AK4	D49	E5	NC	AA3	Vcc2	Y1	Vss	B26
A4	AM34	D0	K34	D50	D2	NC	AC3	Vcc2	AA1	Vss	B28
A5	AK32	D1	G35	D51	F4	NC	AC5	Vcc2	AC1	Vss	H2
A6	AN33	D2	J35	D52	E3	NC	AC35	Vcc2	AE1	Vss	H36
A7	AL33	D3	G33	D53	G5	NC	AD4	Vcc2	AG1	Vss	K2
A8	AM32	D4	F36	D54	E1	NC	AE3	Vcc2	AN9	Vss	K36
A9	AK30	D5	F34	D55	G3	NC	AE35	Vcc2	AN11	Vss	M2
A10	AN31	D6	E35	D56	H4	NC	AL7	Vcc2	AN13	Vss	M36
A11	AL31	D7	E33	D57	J3	NC	AL19	Vcc2	AN15	Vss	P2
A12	AL29	D8	D34	D58	J5	NC	AN1	Vcc2	AN17	Vss	P36
A13	AK28	D9	C37	D59	K4	NC	AN3	Vcc2	AN19	Vss	R2
A14	AL27	D10	C35	D60	L5	NC	AN5	Vcc3	A19	Vss	R36
A15	AK26	D11	B36	D61	L3	NMI	AC33	Vcc3	A21	Vss	T2
A16	AL25	D12	D32	D62	M4	PCD	AG5	Vcc3	A23	Vss	T36
A17	AK24	D13	B34	D63	N3	PCHK#	AF4	Vcc3	A25	Vss	U35
A18	AL23	D14	C33	DP0	D36	PWT	AL3	Vcc3	A27	Vss	V2
A19	AK22	D15	A35	DP1	D30	Reserved	Q3	Vcc3	A29	Vss	V36
A20	AL21	D16	B32	DP2	C25	Reserved	R4	Vcc3	E37	Vss	X2
A20M#	AK8	D17	C31	DP3	D18	Reserved	S3	Vcc3	G37	Vss	X36
A21	AF34	D18	A33	DP4	C7	Reserved	S33	Vcc3	J37	Vss	Z2
A22	AH36	D19	D28	DP5	F6	Reserved	S35	Vcc3	L33	Vss	Z36
A23	AE33	D20	B30	DP6	F2	Reserved	W35	Vcc3	L37	Vss	AB2
A24	AG35	D21	C29	DP7	N5	Reserved	X34	Vcc3	N37	Vss	AB36
A25	AJ35	D22	A31	EADS#	AM4	Reserved	Y35	Vcc3	Q37	Vss	AD2
A26	AH34	D23	D26	EWBE#	W3	Reserved	AN35	Vcc3	S37	Vss	AD36
A27	AG33	D24	C27	FERR#	Q5	RESET	AK20	Vcc3	T34	Vss	AF2
A28	AK36	D25	C23	FLUSH#	AN7	SCYC	AL17	Vcc3	U33	Vss	AF36
A29	AK34	D26	D24	HIT#	AK6	SMI#	AB34	Vcc3	U37	Vss	AH2
A30	AM36	D27	C21	HITM#	AL5	SMIACT#	AG3	Vcc3	W37	Vss	AJ37
A31	AJ33	D28	D22	HLDA	AJ3	SUSP#	V34	Vcc3	Y37	Vss	AL37
ADS#	AJ5	D29	C19	HOLD	AB4	SUSPA#	W33	Vcc3	AA37	Vss	AM8
ADSC#	AM2	D30	D20	IGNNE#	AA35	TCK	M34	Vcc3	AC37	Vss	AM10
AHOLD	V4	D31	C17	INTR	AD34	TDI	N35	Vcc3	AE37	Vss	AM12
AP	AK2	D32	C15	INV	U5	TDO	N33	Vcc3	AG37	Vss	AM14
APCHK#	AE5	D33	D16	KEN#	W5	TMS	P34	Vcc3	AN21	Vss	AM16
BE0#	AL9	D34	C13	LOCK#	AH4	TRST#	Q33	Vcc3	AN23	Vss	AM18
BE1#	AK10	D35	D14	MI/O#	T4	Vcc2	A7	Vcc3	AN25	Vss	AM20
BE2#	AL11	D36	C11	NA#	Y5	Vcc2	A9	Vcc3	AN27	Vss	AM22
BE3#	AK12	D37	D12	NC	A3	Vcc2	A11	Vcc3	AN29	Vss	AM24
BE4#	AL13	D38	C9	NC	A37	Vcc2	A13	Vcc2DET	AL1	Vss	AM26
BE5#	AK14	D39	D10	NC	B2	Vcc2	A15	Vss	B6	Vss	AM28
BE6#	AL15	D40	D8	NC	C1	Vcc2	A17	Vss	B8	Vss	AM30
BE7#	AK16	D41	A5	NC	H43	Vcc2	G1	Vss	B10	Vss	AN37
BOFF#	Z4	D42	E9	NC	J33	Vcc2	J1	Vss	B12	W/R#	AM6
BRDY#	X4	D43	B4	NC	L35	Vcc2	L1	Vss	B14	WB/WT#	AA5
BRDYC#	Y3	D44	D6	NC	P4	Vcc2	N1	Vss	B16	WM_RST	AA33
BREQ	AJ1	D45	C5	NC	Q35	Vcc2	Q1	Vss	B18		
CACHE#	U3	D46	E7	NC	R34	Vcc2	S1	Vss	B20		
CLK	AK18	D47	C3	NC	S5	Vcc2	U1	Vss	B22		
CLKMUL	Y33	D48	D4	NC	Z34	Vcc2	W1	Vss	B24		

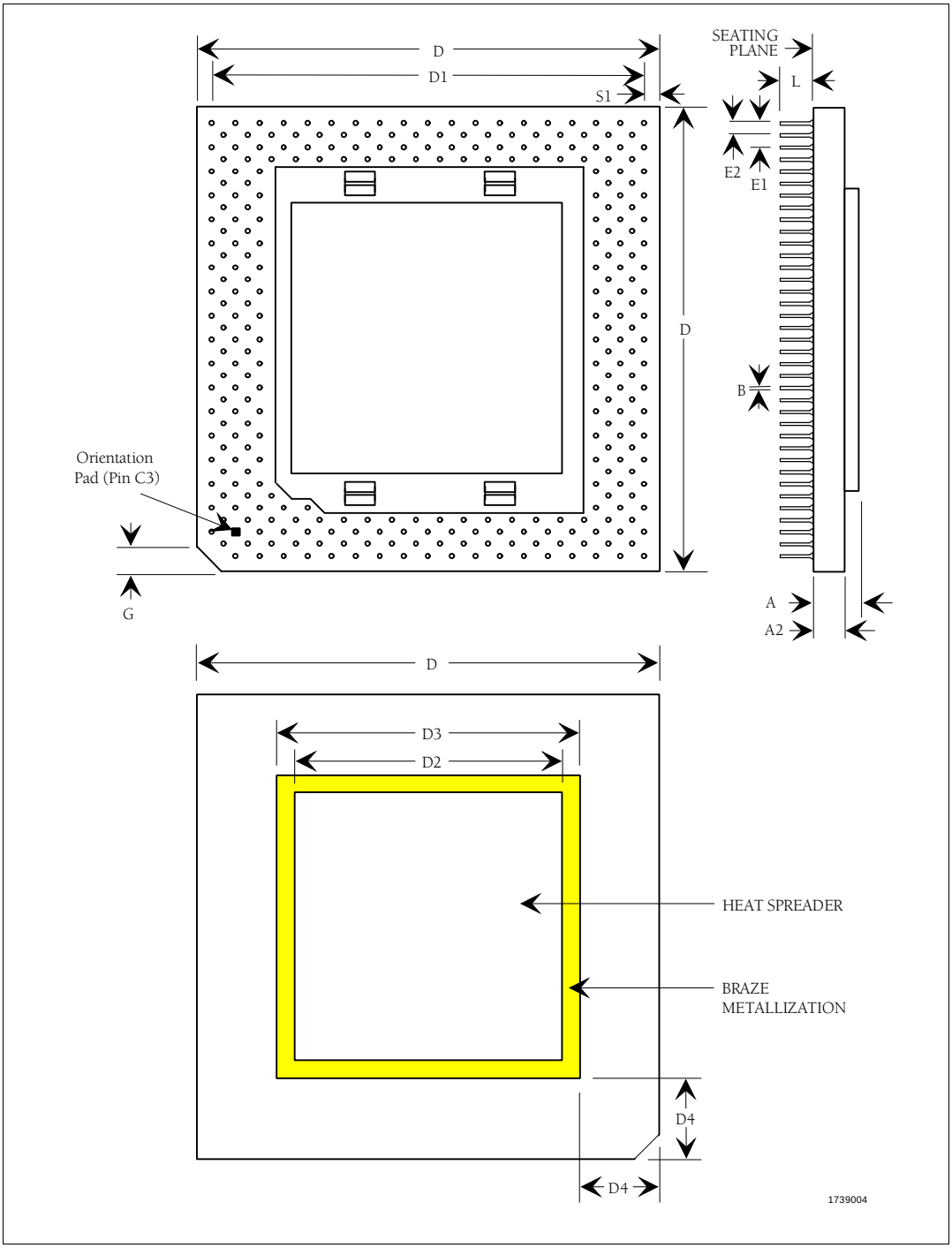

Figure 3-3. 296-Pin SPGA Package (Type C)

Table 3-3. 296-Pin Package (Type C) Dimensions

SYMBOL	MILLIMETERS		INCHES		DESCRIPTION
	MIN	MAX	MIN	MAX	
A	3.43	4.34	0.135	0.171	Distance from seating plane datum to highest point on body.
A2	2.52	3.07	0.099	0.121	Ceramic substrate thickness.
B	0.43	0.51	0.017	0.020	Pin diameter.
D	49.28	49.91	1.940	1.965	Largest overall package length.
D1	45.47	45.97	1.790	1.810	Distance from outer pin center to outer pin center
D2	31.50	32.00	1.240	1.260	Longest side of metal heat spreader.
D3	33.99	34.59	1.338	1.362	Longest side of braze metallization.
D4	8.00	9.91	0.315	0.390	Minimum distance from braze metallization to substrate edge.
E1	2.41	2.67	0.095	0.105	Linear spacing between true pin position centerlines.
E2	1.14	1.40	0.045	0.055	Diagonal spacing between true pin centerlines.
F	-	0.127	-	0.005	Flatness of heat spreader, measured diagonally.
G	1.52	2.29	0.060	0.090	Vertical distance for 45° chamfer index corner
L	2.97	3.38	0.117	0.133	Distance from seating plane to tip of pin.
S1	1.65	2.16	0.065	0.085	Distance from outer pin center to edge of body.