

#### 4.0 ELECTRICAL SPECIFICATIONS

##### 4.1 Electrical Connections

This section provides information on electrical connections, absolute maximum ratings, recommended operating conditions, DC characteristics, and AC characteristics. All voltage values in Electrical Specifications are measured with respect to  $V_{SS}$  unless otherwise noted.

##### 4.1.1 Power and Ground Connections and Decoupling

Testing and operating the IBM 6x86 CPU requires the use of standard high frequency techniques to reduce parasitic effects. The high clock frequencies used in the IBM 6x86 CPU and its output buffer circuits can cause transient power surges when several output buffers switch output levels simultaneously. These effects can be minimized by filtering the DC power leads with low-inductance decoupling capacitors, using low impedance wiring, and by utilizing all of the  $V_{CC}$  and GND pins. The IBM 6x86 CPU contains 296 pins with 53 pins connected to  $V_{CC}$  and 53 connected to  $V_{SS}$  (ground).

##### 4.1.2 Pull-Up/Pull-Down Resistors

Table 4-1 lists the input pins that are internally connected to pull-up and pull-down resistors. The pull-up resistors are connected to  $V_{CC}$  and the pull-down resistors are connected to  $V_{SS}$ . When unused, these inputs do not require connection to external pull-up or pull-down resistors. The SUSP# pin is unique in that it is connected to a pull-up resistor only when SUSP# is not asserted.

Table 4-1. Pins Connected to Internal Pull-Up and Pull-Down Resistors

SIGNAL	PIN NO.	RESISTOR
BRDYC#	Y3	20-k $\Omega$ pull-up
CLKMUL	Y33	20-k $\Omega$ pull-down
QDUMP#	AL7	20-k $\Omega$ pull-up
SMI#	AB34	
SUSP#	V34	20-k $\Omega$ pull-up (see text)
TCK	M34	20-k $\Omega$ pull-up
TDI	N35	
TMS	P34	
TRST#	Q33	
Reserved	J33	
Reserved	W35	
Reserved	Y35	
Reserved	AN35	20-k $\Omega$ pull-down



#### 4.1.3 Unused Input Pins

All inputs not used by the system designer and not listed in Table 4-1 should be connected either to ground or to  $V_{CC}$ . Connect active-high inputs to ground through a 20 k $\Omega$  ( $\pm 10\%$ ) pull-down resistor and active-low inputs to  $V_{CC}$  through a 20 k $\Omega$  ( $\pm 10\%$ ) pull-up resistor to prevent possible spurious operation.

#### 4.1.4 NC and Reserved Pins

Pins designated NC have no internal connections. Pins designated RESV or RESERVED should be left disconnected. Connecting a reserved pin to a pull-up resistor, pull-down resistor, or an active signal could cause unexpected results and possible circuit malfunctions.

#### 4.2 Absolute Maximum Ratings

The following table lists absolute maximum ratings for the IBM 6x86 CPU microprocessors. Stresses beyond those listed under Table 4-2 limits may cause permanent damage to the device. These are stress ratings only and do not imply that operation under any conditions other than those listed under "Recommended Operating Conditions" Table 4-3 (Page 4-3) is possible. Exposure to conditions beyond Table 4-2 may (1) reduce device reliability and (2) result in premature failure even when there is no immediately apparent sign of failure. Prolonged exposure to conditions at or near the absolute maximum ratings may also result in reduced useful life and reliability.

Table 4-2. Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNITS	NOTES
Storage Temperature	-65	150	$^{\circ}\text{C}$	
Supply Voltage, $V_{CC}$	-0.5	4.0	V	
Voltage On Any Pin	-0.5	$V_{CC}+0.5$	V	
Input Clamp Current, $I_{IK}$		10	mA	Power Applied
Output Clamp Current, $I_{OK}$		25	mA	Power Applied

### 4.3 Recommended Operating Conditions

Table 4-3 presents the recommended operating conditions for the IBM 6x86 CPU device.

**Table 4-3. Recommended Operating Conditions**

PARAMETER	MIN	MAX	UNITS	NOTES
T <sub>C</sub> Operating Case Temperature	0	75	°C	Power Applied
V <sub>CC</sub> =3.3V <sub>nom</sub> , Supply Voltage	3.15	3.6	V	
V <sub>CC</sub> =3.5V <sub>nom</sub> , Supply Voltage	3.4	3.6	V	
V <sub>IH</sub> High-Level Input Voltage	2.0	5.5	V	
V <sub>IL</sub> Low-Level Input Voltage	-0.3	0.8	V	
I <sub>OH</sub> High-Level Output Current, All outputs		-1.0	mA	V <sub>O</sub> =V <sub>OH(MIN)</sub>
I <sub>OL</sub> Low-Level Output Current, All outputs		5.0	mA	V <sub>O</sub> =V <sub>OL(MAX)</sub>



4.4 DC Characteristic

Table 4-4. DC Characteristics (at Recommended Operating Conditions)

PARAMETER	MIN	TYP	MAX	UNIT S	NOTES
V <sub>OL</sub> Output Low Voltage I <sub>OL</sub> = 5 mA			0.4	V	
V <sub>OH</sub> Output High Voltage I <sub>OH</sub> = -1 mA	2.4			V	
I <sub>I</sub> Input Leakage Current For all pins except those listed in Table 4-1.			±15	µA	0 < V <sub>IN</sub> < V <sub>CC</sub>
I <sub>IH</sub> Input Leakage Current For all pins with internal pull-downs.			200	µA	V <sub>IH</sub> = 2.4 V See Table 4-1.
I <sub>IL</sub> Input Leakage Current For all pins with internal pull-ups.			-400	µA	V <sub>IL</sub> = 0.45 V See Table 4-1.
I <sub>CC</sub> 100 MHz 110 MHz 120 MHz 133 MHz 150 MHz		4500 4800 5100 5500 6000	5400 5800 6100 6600 7000	mA	Note 1, 5, 6
I <sub>CCSM</sub> (Suspend Mode I <sub>CC</sub> ) 100 MHz 110 MHz 120 MHz 133 MHz 150 MHz		48 50 51 54 60	80 83 105 115 125	mA	Note 1, 3, 5
I <sub>CCSS</sub> Standby I <sub>CC</sub> 0 MHz (Suspended/CLK Stopped)		35	55	mA	Note 4,5
C <sub>IN</sub> Input Capacitance			15	pF	f = 1 MHz, Note 2
C <sub>OUT</sub> Output Capacitance			20	pF	f = 1 MHz, Note 2
C <sub>IO</sub> I/O Capacitance			25	pF	f = 1 MHz, Note 2
C <sub>CLK</sub> CLK Capacitance			15	pF	f = 1 MHz, Note 2

Notes:

1. Frequency (MHz) ratings refer to the internal clock frequency.
2. Not 100% tested.
3. All inputs at 0.4 or V<sub>CC</sub> - 0.4 (CMOS levels). All inputs held static except clock and all outputs unloaded (static I<sub>OUT</sub> = 0 mA).
4. All inputs at 0.4 or V<sub>CC</sub> - 0.4 (CMOS levels). All inputs held static and all outputs unloaded (static I<sub>OUT</sub> = 0 mA).
5. Typical, measured at V<sub>CC</sub> = 3.3 V
6. Max, measured at V<sub>CC</sub>=3.6V. Lab Testing on some devices has produced Max current draws of:  
 100MHz....6.05A  
 110MHz....6.58A  
 120MHz....6.95A  
 133MHz....7.50A  
 150MHz....7.11A

#### 4.5 AC Characteristics

Tables 4-6 through 4-11 (Pages 4-7 through 4-13) list the AC characteristics including output delays, input setup requirements, input hold requirements and output float delays. These measurements are based on the measurement points identified in Figure 4-1 (Page 4-6) and Figure 4-2 (Page 4-7). The rising clock edge reference level  $V_{REF}$  and other reference levels

are shown in Table 4-5. Input or output signals must cross these levels during testing.

Figure 4-1 shows output delay (A and B) and input setup and hold times (C and D). Input setup and hold times (C and D) are specified minimums, defining the smallest acceptable sampling window a synchronous input signal must be stable for correct operation.

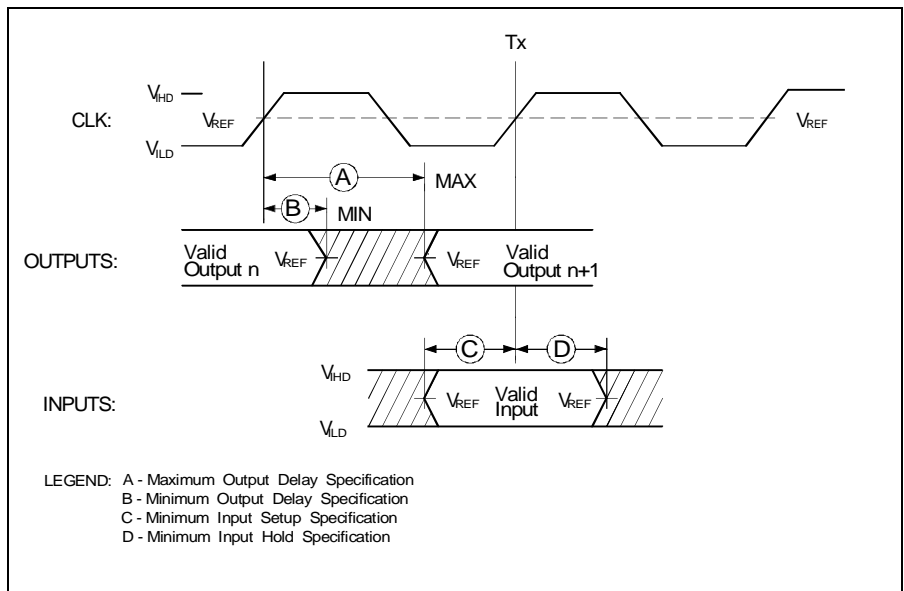


Figure 4-1. Drive Level and Measurement Points for Switching Characteristics.

Table 4-5. Drive Level and Measurement Points for Switching Characteristics

SYMBOL	VOLTAGE (Volts)
$V_{REF}$	1.5
$V_{IHD}$	2.3
$V_{ILD}$	0

Note: Refer to Figure 4-1.

Table 4-6. Clock Specifications  
 $T_{CASE} = 0^{\circ}C$  to  $75^{\circ}C$ , See Figure 4-2

SYMBOL	PARAMETER	50-MHz BUS		55-MHz BUS		60-MHz BUS		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
	CLK Frequency		50.0		55.0		60.0	MHz
T1	CLK Period	20.0		18.0		16.67		ns
T2	CLK Period Stability		$\pm 250$		$\pm 250$		$\pm 250$	ps
T3	CLK High Time	7.00		4.00		4.00		ns
T4	CLK Low Time	7.00		4.00		4.00		ns
T5	CLK Fall Time	0.15	2.00	0.15	1.50	0.15	1.50	ns
T6	CLK Rise Time	0.15	2.00	0.15	1.50	0.15	1.50	ns

SYMBOL	PARAMETER	66-MHz BUS		75-MHz BUS		UNITS
		MIN	MAX	MIN	MAX	
	CLK Frequency		66.6		75.0	MHz
T1	CLK Period	15.0		13.3		ns
T2	CLK Period Stability		$\pm 250$		$\pm 250$	ps
T3	CLK High Time	4.00		4.00		ns
T4	CLK Low Time	4.00		4.00		ns
T5	CLK Fall Time	0.15	1.50	0.15	1.50	ns
T6	CLK Rise Time	0.15	1.50	0.15	1.50	ns

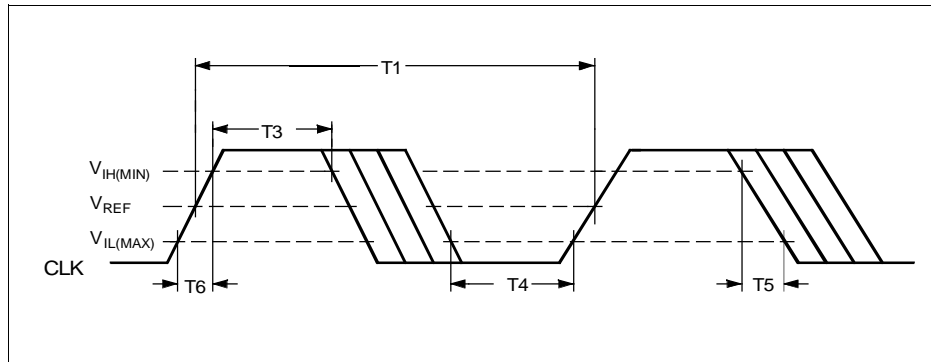


Figure 4-2. CLK Timing and Measurement Points



**Table 4-7. Output Valid Delays**  
**CL=50 pF, TCASE =0°C to 75°C, See Figure 4-3**

SYMBOL	PARAMETER	50MHz BUS		55MHz BUS		60-MHz BUS		66-MHz BUS		75MHz BUS		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
T7a	A31-A3, BE7#-BE0#, CACHE#, D/C#, LBA#, LOCK#, PCD, PWT, SCYC, SMIACT#, W/R#	1	12	1.0	7.0	1.0	7.0	1.0	7.0	1.0	7.0	ns
T7b	ADS#, M/IO#	1	12	1.0	7.0	1.0	7.0	1.0	6.0	1.0	6.0	ns
T8	ADSC#	1	12	1.0	7.0	1.0	7.0	1.0	7.0	1.0	7.0	ns
T9	AP	1	12	1.0	8.5	1.0	8.5	1.0	8.5	1.0	8.5	ns
T10	APCHK#, PCHK#, FERR#	1	14	1.0	8.3	1.0	7.0	1.0	7.0	1.0	7.0	ns
T11	D63-D0, DP7-DP0 (Write)	1.3	12	1.3	8.5	1.3	7.5	1.3	7.5	1.0	7.5	ns
T12a	HIT#	1	12	1.0	8.0	1.0	8.0	1.0	8.0	1.0	8.0	ns
T12b	HITM#	1.1	12	1.1	6.0	1.1	6.0	1.1	6.0	1.0	6.0	ns
T13	BREQ, HLDA	1	12	1.0	8.0	1.0	8.0	1.0	8.0	1.0	8.0	ns
T14	SUSPA#	1	14	1.0	8.0	1.0	8.0	1.0	8.0	1.0	8.0	ns

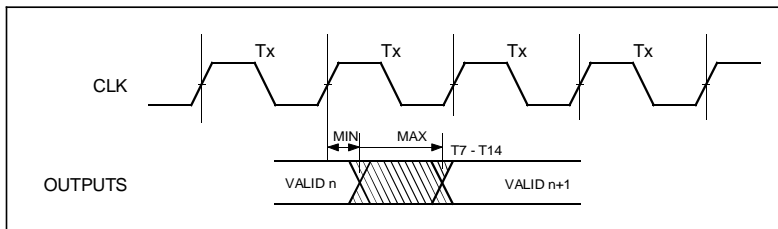


Figure 4-3. Output Valid Delay Timing.



**Table 4-8. Output Float Delays**  
 $C_L = 50 \text{ pF}$ ,  $T_{\text{case}} = 0^\circ\text{C to } 75^\circ\text{C}$ , See Figure 4-5

SYMBOL	PARAMETER	50MHz BUS		55MHz BUS		60MHz BUS		66MHz BUS		75MHz BUS		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
T15	A31-A3, ADS#, BE7#-BE0#, BREQ, CACHE#, D/C#, LBA#, LOCK#, M/IO#, PCD, PWT, SCYC, SMIACT#, W/R#		16.0		10.0		10.0		10.0		10.0	ns
T16	AP		16.0		10.0		10.0		10.0		10.0	ns
T17	D63-D0, DP7-DP0 (Write)		16.0		10.0		10.0		10.0		10.0	ns

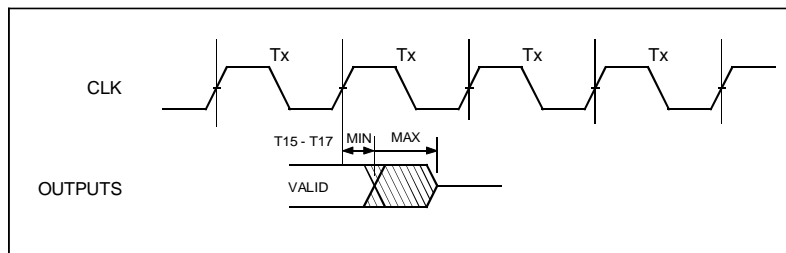


Figure 4-4. Output Float Delay Timing