



296-Pin SPGA Package

Table 5-1. 296-Pin SPGA Package Signal Names Sorted by Pin Number

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A3	NC	C29	D21	J35	D2	U35	Vss	AE35	NC	AL21	A20
A5	D41	C31	D17	J37	Vcc	U37	Vcc	AE37	Vcc	AL23	A18
A7	Vcc	C33	D14	K2	Vss	V2	Vss	AF2	Vss	AL25	A16
A9	Vcc	C35	D10	K4	D59	V4	AHOLD	AF4	PCHK#	AL27	A14
A11	Vcc	C37	D9	K34	D0	V34	SUSP#	AF34	A21	AL29	A12
A13	Vcc	D2	D50	K36	Vss	V36	Vss	AF36	Vss	AL31	A11
A15	Vcc	D4	D48	L1	Vcc	W1	Vcc	AG1	Vcc	AL33	A7
A17	Vcc	D6	D44	L3	D61	W3	EWBE#	AG3	SMIACT#	AL35	A3
A19	Vcc	D8	D40	L5	D60	W5	KEN#	AG5	PCD	AL37	Vss
A21	Vcc	D10	D39	L33	Vcc	W33	SUSPA#	AG33	A27	AM2	ADSC#
A23	Vcc	D12	D37	L35	NC	W35	Reserved	AG35	A24	AM4	EADS#
A25	Vcc	D14	D35	L37	Vcc	W37	Vcc	AG37	Vcc	AM6	W/R#
A27	Vcc	D16	D33	M2	Vss	X2	Vss	AH2	Vss	AM8	Vss
A29	Vcc	D18	DP3	M4	D62	X4	BRDY#	AH4	LOCK#	AM10	Vss
A31	D22	D20	D30	M34	TCK	X34	Reserved	AH34	A26	AM12	Vss
A33	D18	D22	D28	M36	Vss	X36	Vss	AH36	A22	AM14	Vss
A35	D15	D24	D26	N1	Vcc	Y1	Vcc	AJ1	BREQ	AM16	Vss
A37	NC	D26	D23	N3	D63	Y3	BRDYC#	AJ3	HLDA	AM18	Vss
B2	NC	D28	D19	N5	DP7	Y5	NA#	AJ5	ADS#	AM20	Vss
B4	D43	D30	DP1	N33	TDO	Y33	CLKMUL	AJ33	A31	AM22	Vss
B6	Vss	D32	D12	N35	TDI	Y35	Reserved	AJ35	A25	AM24	Vss
B8	Vss	D34	D8	N37	Vcc	Y37	Vcc	AJ37	Vss	AM26	Vss
B10	Vss	D36	DP0	P2	Vss	Z2	Vss	AK2	AP	AM28	Vss
B12	Vss	E1	D54	P4	NC	Z4	BOFF#	AK4	D/C#	AM30	Vss
B14	Vss	E3	D52	P34	TMS	Z34	NC	AK6	HIT#	AM32	A8
B16	Vss	E5	D49	P36	Vss	Z36	Vss	AK8	A20M#	AM34	A4
B18	Vss	E7	D46	Q1	Vcc	AA1	Vcc	AK10	BE1#	AM36	A30
B20	Vss	E9	D42	Q3	Reserved	AA3	Reserved	AK12	BE3#	AN1	NC
B22	Vss	E33	D7	Q5	FERR#	AA5	WB/WT#	AK14	BE5#	AN3	NC
B24	Vss	E35	D6	Q33	TRST#	AA33	WM_RST	AK16	BE7#	AN5	NC
B26	Vss	E37	Vcc	Q35	NC	AA35	IGNNE#	AK18	CLK	AN7	FLUSH#
B28	Vss	F2	DP6	Q37	Vcc	AA37	Vcc	AK20	RESET	AN9	Vcc
B30	D20	F4	D51	R2	Vss	AB2	Vss	AK22	A19	AN11	Vcc
B32	D16	F6	DP5	R4	Reserved	AB4	HOLD	AK24	A17	AN13	Vcc
B34	D13	F34	D5	R34	BHOLD	AB34	SMI#	AK26	A15	AN15	Vcc
B36	D11	F36	D4	R36	Vss	AB36	Vss	AK28	A13	AN17	Vcc
C1	NC	G1	Vcc	S1	Vcc	AC1	Vcc	AK30	A9	AN19	Vcc
C3	D47	G3	D55	S3	Reserved	AC3	Reserved	AK32	A5	AN21	Vcc
C5	D45	G5	D53	S5	LBA#	AC5	NC	AK34	A29	AN23	Vcc
C7	DP4	G33	D3	S33	Reserved	AC33	NMI	AK36	A28	AN25	Vcc
C9	D38	G35	D1	S35	DHOLD	AC35	NC	AL1	NC	AN27	Vcc
C11	D36	G37	Vcc	S37	Vcc	AC37	Vcc	AL3	PWT	AN29	Vcc
C13	D34	H2	Vss	T2	Vss	AD2	Vss	AL5	HITM#	AN31	A10
C15	D32	H4	D56	T4	MI/O#	AD4	NC	AL7	QDUMP#	AN33	A6
C17	D31	H34	NC	T34	Vcc	AD34	INTR	AL9	BE0#	AN35	Reserved
C19	D29	H36	Vss	T36	Vss	AD36	Vss	AL11	BE2#	AN37	Vss
C21	D27	J1	Vcc	U1	Vcc	AE1	Vcc	AL13	BE4#		
C23	D25	J3	D57	U3	CACHE#	AE3	NC	AL15	BE6#		
C25	DP2	J5	D58	U5	INV	AE5	APCHK#	AL17	SCYC		
C27	D24	J33	Reserved	U33	Vcc	AE33	A23	AL19	Reserved		

Note: Reserved pins are reserved for future use by IBM only. Pins marked NC are not internally connected.

Table 5-2. 296-Pin SPGA Package Pin Numbers Sorted by Signal Name

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
A3	AL35	CLKMUL	Y33	D48	D4	NC	AN3	Vcc	AA37	Vss	AM12
A4	AM34	D/C#	AK4	D49	E5	NC	AN5	Vcc	AC1	Vss	AM14
A5	AK32	D0	K34	D50	D2	NC	B2	Vcc	AC37	Vss	AM16
A6	AN33	D1	G35	D51	F4	NC	C1	Vcc	AE1	Vss	AM18
A7	AL33	D2	J35	D52	E3	NC	H34	Vcc	AE37	Vss	AM20
A8	AM32	D3	G33	D53	G5	NC	L35	Vcc	AG1	Vss	AM22
A9	AK30	D4	F36	D54	E1	NC	P4	Vcc	AG37	Vss	AM24
A10	AN31	D5	F34	D55	G3	NC	Q35	Vcc	AN11	Vss	AM26
A11	AL31	D6	E35	D56	H4	NC	Z34	Vcc	AN13	Vss	AM28
A12	AL29	D7	E33	D57	J3	NMI	AC33	Vcc	AN15	Vss	AM30
A13	AK28	D8	D34	D58	J5	PCD	AG5	Vcc	AN17	Vss	AM8
A14	AL27	D9	C37	D59	K4	PCHK#	AF4	Vcc	AN19	Vss	AN37
A15	AK26	D10	C35	D60	L5	PWT	AL3	Vcc	AN21	Vss	B6
A16	AL25	D11	B36	D61	L3	QDUMP#	AL7	Vcc	AN23	Vss	B8
A17	AK24	D12	D32	D62	M4	RESET	AK20	Vcc	AN25	Vss	B10
A18	AL23	D13	B34	D63	N3	SCYC	AL17	Vcc	AN27	Vss	B12
A19	AK22	D14	C33	DHOLD	S35	Reserved	AA3	Vcc	AN29	Vss	B14
A20	AL21	D15	A35	DP0	D36	Reserved	AC3	Vcc	AN9	Vss	B16
A20M#	AK8	D16	B32	DP1	D30	Reserved	AL19	Vcc	E37	Vss	B18
A21	AF34	D17	C31	DP2	C25	Reserved	AN35	Vcc	G1	Vss	B20
A22	AH36	D18	A33	DP3	D18	Reserved	J33	Vcc	G37	Vss	B22
A23	AE33	D19	D28	DP4	C7	Reserved	Q3	Vcc	J1	Vss	B24
A24	AG35	D20	B30	DP5	F6	Reserved	R4	Vcc	J37	Vss	B26
A25	AJ35	D21	C29	DP6	F2	Reserved	S3	Vcc	L1	Vss	B28
A26	AH34	D22	A31	DP7	N5	Reserved	S33	Vcc	L33	Vss	H2
A27	AG33	D23	D26	EADS#	AM4	Reserved	W35	Vcc	L37	Vss	H36
A28	AK36	D24	C27	EWBE#	W3	Reserved	X34	Vcc	N1	Vss	K2
A29	AK34	D25	C23	FERR#	Q5	Reserved	Y35	Vcc	N37	Vss	K36
A30	AM36	D26	D24	FLUSH#	AN7	SMI#	AB34	Vcc	Q1	Vss	M2
A31	AJ33	D27	C21	HIT#	AK6	SMIACT#	AG3	Vcc	Q37	Vss	M36
ADS#	AJ5	D28	D22	HITM#	AL5	SUSP#	V34	Vcc	S1	Vss	P2
ADSC#	AM2	D29	C19	HLDA	AJ3	SUSPA#	W33	Vcc	S37	Vss	P36
AHOLD	V4	D30	D20	HOLD	AB4	TCK	M34	Vcc	T34	Vss	R2
AP	AK2	D31	C17	IGNNE#	AA35	TDI	N35	Vcc	U1	Vss	R36
APCHK#	AE5	D32	C15	INTR	AD34	TDO	N33	Vcc	U33	Vss	T2
BE0#	AL9	D33	D16	INV	U5	TMS	P34	Vcc	U37	Vss	T36
BE1#	AK10	D34	C13	KEN#	W5	TRST#	Q33	Vcc	W1	Vss	U35
BE2#	AL11	D35	D14	LBA#	S5	Vcc	A7	Vcc	W37	Vss	V2
BE3#	AK12	D36	C11	LOCK#	AH4	Vcc	A9	Vcc	Y1	Vss	V36
BE4#	AL13	D37	D12	MI/O#	T4	Vcc	A11	Vcc	Y37	Vss	X2
BE5#	AK14	D38	C9	NA#	Y5	Vcc	A13	Vss	AB2	Vss	X36
BE6#	AL15	D39	D10	NC	A3	Vcc	A15	Vss	AB36	Vss	Z2
BE7#	AK16	D40	D8	NC	A37	Vcc	A17	Vss	AD2	Vss	Z36
BHOLD	R34	D41	A5	NC	AC35	Vcc	A19	Vss	AD36	WB/WT#	AA5
BOFF#	Z4	D42	E9	NC	AC5	Vcc	A21	Vss	AF2	W/R#	AM6
BRDY#	X4	D43	B4	NC	AD4	Vcc	A23	Vss	AF36	WM_RST	AA33
BRDYC#	Y3	D44	D6	NC	AE3	Vcc	A25	Vss	AH2		
BREQ	AJ1	D45	C5	NC	AE35	Vcc	A27	Vss	AJ37		
CACHE#	U3	D46	E7	NC	AL1	Vcc	A29	Vss	AL37		
CLK	AK18	D47	C3	NC	AN1	Vcc	AA1	Vss	AM10		

Note: Reserved pins are reserved for future use by IBM only. Pins marked NC are not internally connected.



296-Pin SPGA Package

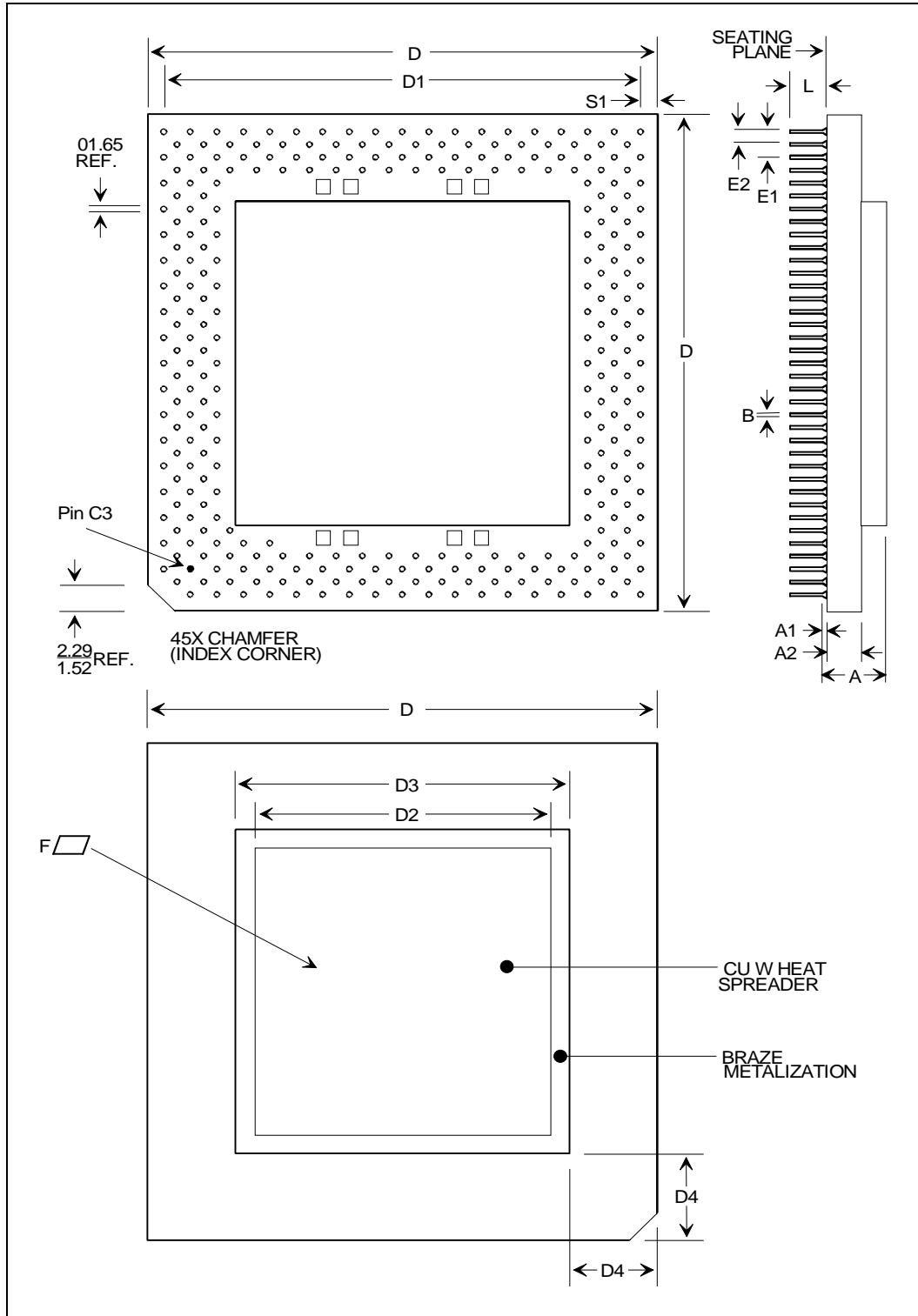


Figure 5-2. 296-Pin SPGA Package

Table 5-3. 296-Pin SPGA Package Dimensions

SYMBOL	MILLIMETERS	
	MIN	MAX
A	3.00	4.20
A1	0.63	1.04
A2	2.51	3.10
B	0.43	0.51
D	49.28	49.91
D1	45.47	45.97
D2	31.50 Sq.	32.00 Sq.
D3	33.91	36.49
D4	6.39	8.00
E1	2.41	2.67
E2	1.14	1.40
F	0.05 Diag.	0.08 Diag.
L	3.05	3.30
N	296 (Pin Count)	
S1	1.47	2.39



5.2 Thermal Characteristics

The IBM 6x86 processor is designed to operate when the case temperature at the top center of the package is between 0°C and 70°C. The maximum die (junction) temperature, $T_{J\text{MAX}}$, and the maximum ambient temperature, $T_{A\text{MAX}}$, can be calculated by substituting thermal resistance and maximum values for case or junction temperature and power dissipation in the following equations:

$$\begin{aligned} T_J &= T_C + (P * \theta_{JC}) \\ T_A &= T_J - (P * \theta_{JA}) \end{aligned}$$

where:

- T_A = Ambient temperature (°C)
- T_J = Average junction temperature (°C)
- T_C = Case temperature at top center of package (°C)
- P = Power dissipation (W)
- θ_{JC} = Junction-to-case thermal resistance (°C/W)
- θ_{JA} = Junction-to-ambient thermal resistance (°C/W).

Table 5-4 lists the junction-to-case and case-to-ambient thermal resistances for the SPGA package.

**Table 5-4. Thermal Resistances for SPGA
Package With and Without Heatsinks**

Thermal Resistance	θ_{JC} °C/W	θ_{CA} °C/W					
		0	100	200	400	600	800
Laminar Air Flow (ft/min)	0	0	100	200	400	600	800
1.95 x 1.95 x 0.25 Heatsink	0.9	8.4	7.4	6.0	4.0	3.1	2.6
1.95 x 1.95 x 0.40 Heatsink	0.9	7.7	6.6	4.9	3.2	2.7	2.1
1.95 x 1.95 x 0.65 Heatsink	0.9	5.9	4.7	3.2	2.1	1.7	1.4
Without Heatsink	1.4	14.7	11.5	9.1	7.3	7.0	6.2

Notes:

For a 6x86 processor with 1.25 x 1.25 x 0.40 inch CuW heat spreader.

Heatsinks are omni-directional pin aluminum alloy.

Features are based on standard extrusion practices for a given height.

Heatsink attachment was made with 0.006 inch of thermal grease applied between heatsink and case.

Maximum air temperature is assumed to be 40 °C

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