
IDT WinChip™


# The Windows Microprocessor

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Background

The New IDT WinChip 2

- Used to Be The WinChip “C6+”
- It’s Better Than We Said At MP Forum

“What’s Next” Analysis

Future Roadmap

# IDT WinChip Background

- Announced IDT WinChip C6 Processor 5/97
  - P55-Compatible (includes MMX™ )
  - Developed by Centaur (IDT Subsidiary)
- Targeting The Value Market
  - Sub-$1000 Desktops & < $1500 Mobile
- Our Strategy: *The Best Value!*
  - Adequate performance (business focus)
  - Unique design → 88-mm$^2$ 4LM die
    → lowest cost → lowest price ≈ ***$50 for 200 MHz***
- 200, 225 & 240 MHz Shipping Now
- >100K Shipped Last Qtr, 2-3x This Qtr

MMX is a trademark of Intel Corporation

# The New IDT WinChip 2

- Significant Performance Improvements per MHz
  - 2x WinChip C6 MMX performance (= P55)
  - 2x WinChip C6 FP performance (> AMD K6)
  - +10% Winstone 98 performance
- Includes 3DNow!™ (AMD Compatible)
  - Significant 3D-graphics performance improvement
- AMD-Compatible 100 MHz Bus (Super7™)
- Multiple Technologies & Fabs
  - IDT 0.35µ & 0.25µ (2 Fabs) + IBM 0.25µ
- Low Cost
  - 95 $mm^2$ vs. 88 for Current WinChip C6 (both 0.35µ)
  - 58 $mm^2$ in IDT 0.25µ ! Smallest in the world !

# IDT WinChip 2 Status

- Sampling Started In April
- First Shipments 7/98
- Versions w/ & w/o 3D Instructions
- Packages
  - Socket 7 CPGA for desktop
  - Special packages for mobile
- MHz Ranges
  - IDT 0.35µ : 225, 240, 266 MHz (July)
  - IDT 0.25µ : 240, 266, 300 MHz (Q3)
  - IBM 0.25µ : 240, 266, 300 MHz (Q4)
- Fractional Bus Multipliers (+3 mos.)

# IDT WinChip 2 MMX & FP

- Full MMX Pairing (Superscalar)
  - Dual MMX Units ala P55 (1 multiplier, 1 shifter)
  - 2 Instructions decoded issued & executed per clock
  - Same pairing rules as P55
  - Same Instruction timings as P55

  *Result: Faster Than K6 & M2 on IMB Image (1x P55)*
- New Fully Pipelined Floating-Point Unit
  - Some instructions slower than P55
  - Some instructions faster

  *Result: Faster Than K6 & M2 on IMB 3D (0.82x P55)*
- We Intentionally Stopped Here!
  - Silicon better spent on 3D instructions

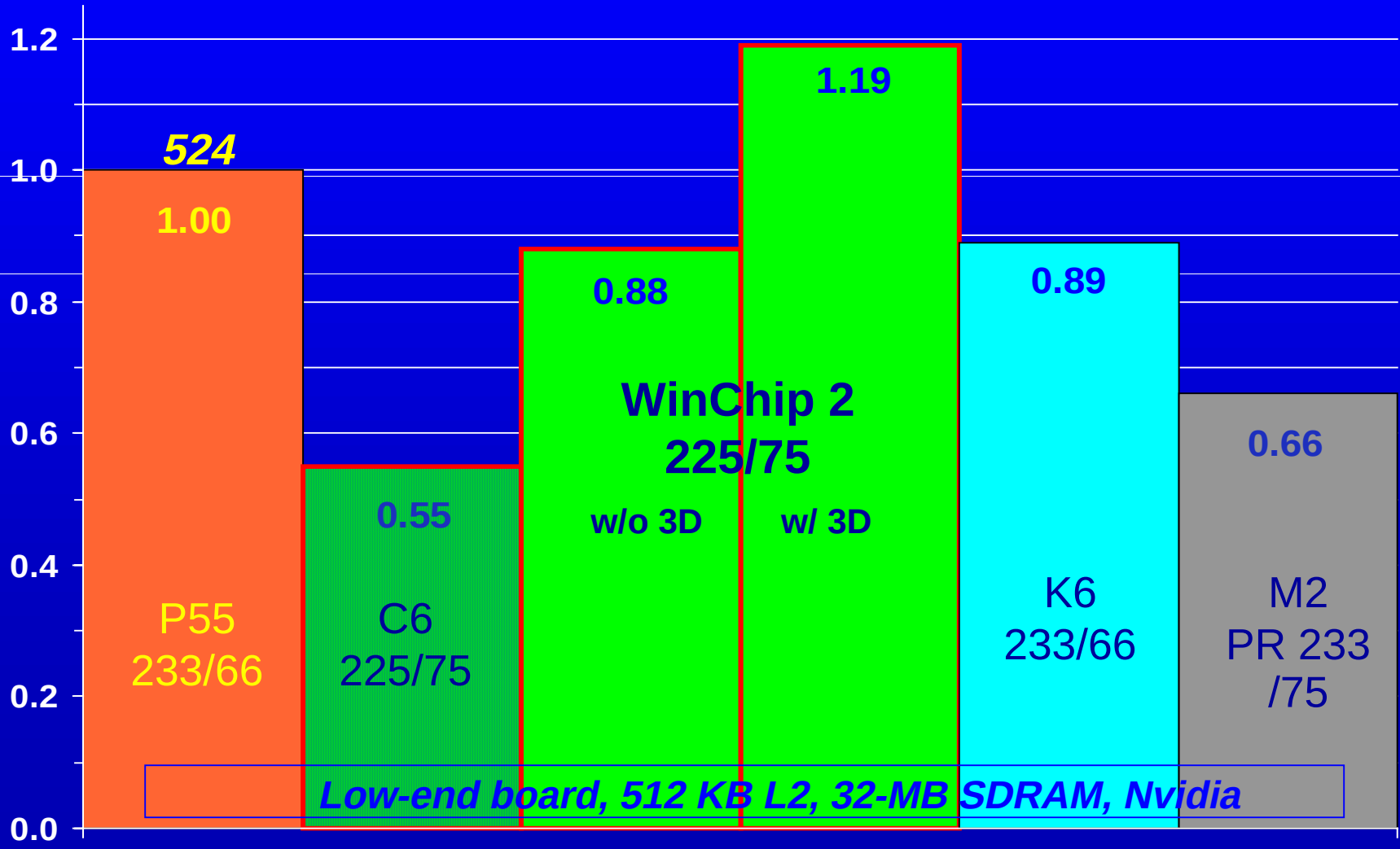
# IDT WinChip 2 3D

- AMD Compatible (Licensed from AMD)
  - Fully compatible with software for AMD K6-3D
- 21 New x86 3D Instructions
  - Plus 4 additional MMX instructions
- Same 3D Instruction Timing As AMD K6-3D Including dual issue add & multiply (superscalar)
  - Except slightly slower on reciprocal & pairing
- Significant Benefits To 3D Gaming

*Result: +32% on 3D Winbench 98*
*Result: +35% on IMB 3D = 1.19x P55*

*(using DirectX 6.0 alpha)*

# WinChip 2 3D Performance

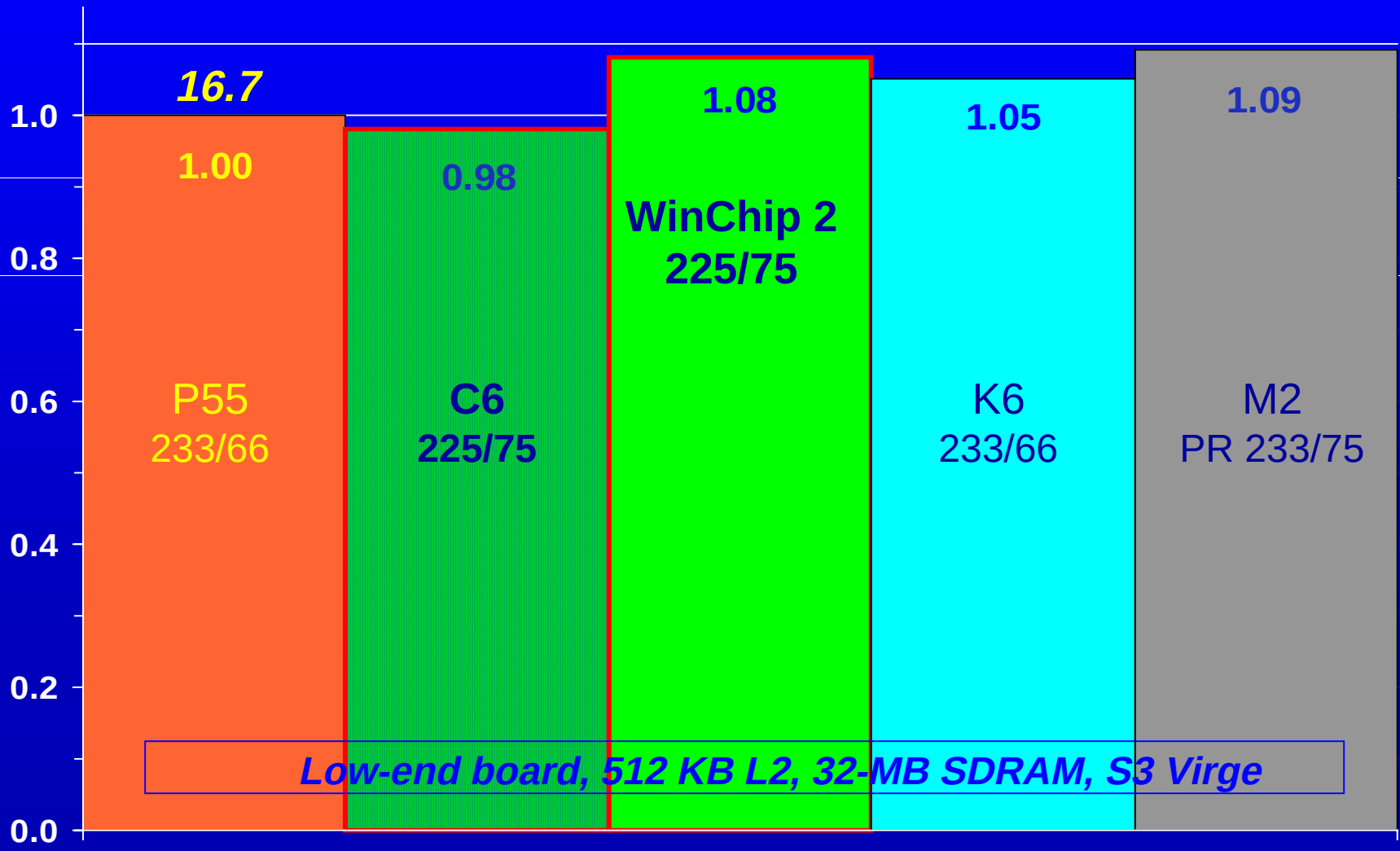



*3D Winbench 98 for Windows 95 w/ DirectX 6.0 (Alpha)*

# WinChip 2 Business Performance

- Doubled TLB Sizes
  - 2x 128 entry (4-way)
- 4-Way D-Cache (vs. 2-Way)
- Many Miscellaneous Improvements
  - Multiply (11 → 6)
  - Load-ALU-Store (3 → 2)
  - No penalty for 0F prefixes
  - No penalty on base+index
  - Generate Up to 4 Micro Instructions per Clock
- Great Branch Prediction
  - Better performance & much smaller than P55

# WinChip 2 Business Performance

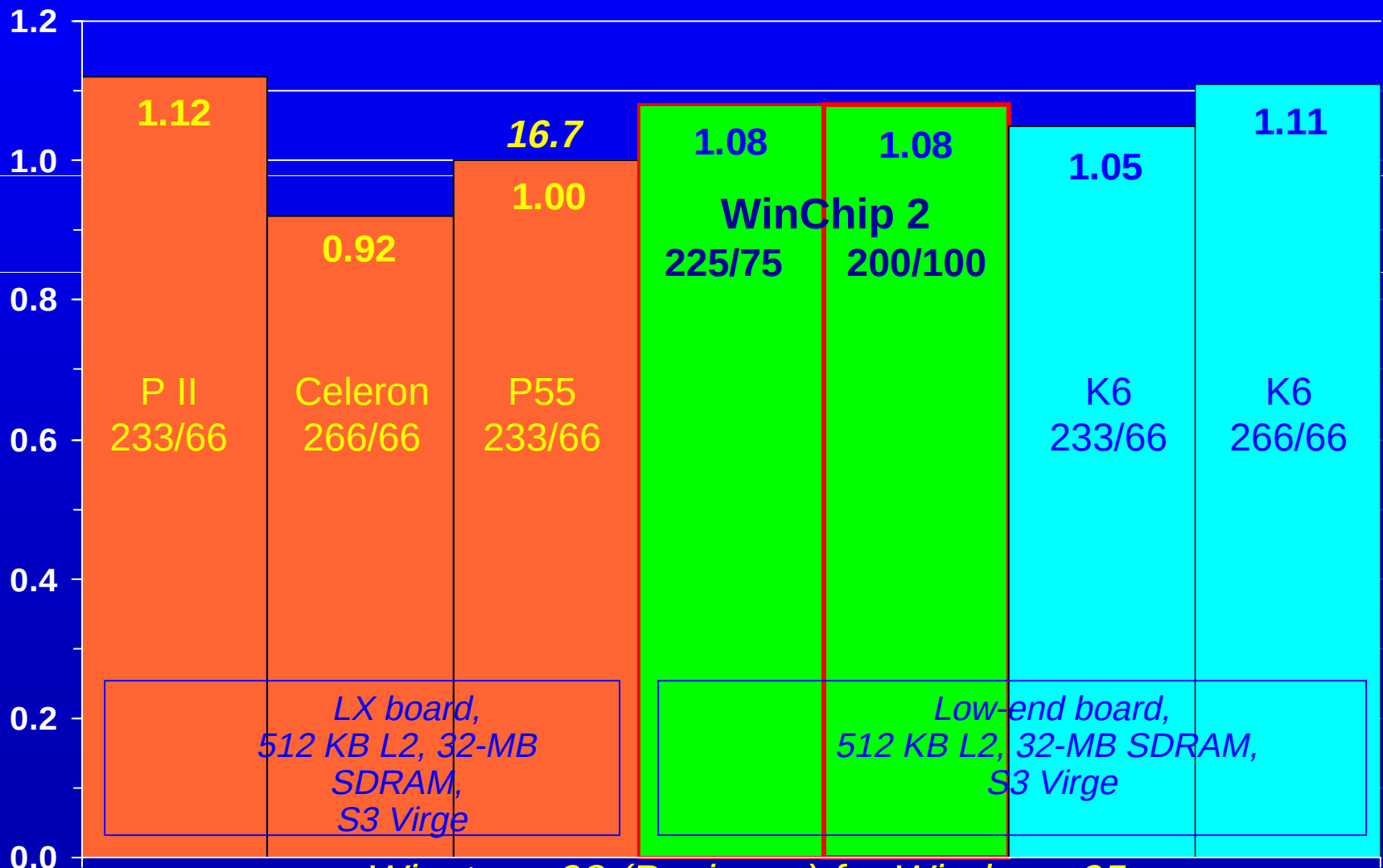



*Winstone 98 (Business) for Windows 95*

# The Emperor Has No Clothes

- MHz Not A Good Indicator Of Real Performance
  - Every processor gets different performance
  - Different applications affected differently
  - eg, Celeron-266
    *slower than any other 200 MHz on WS 98*
- Increasing MHz Yields Small Performance Gain
  - Especially for business applications
  - eg, *P55-233 4% faster than P55-200 on WS 98*
- Bus MHz As Important As Processor MHz
  - eg, *WInChip 200/100 MHz is 6% faster than 200/66*
    (more gain than going to 225 MHz)

# WinChip 2 Business Performance




*Winstone 98 (Business) for Windows 95*

# How To Improve Performance

1. Do More Work per Clock Cycle
   - Superscalar, more functional units, etc.
2. Reduce Bus Stalls
   - Bigger caches & bigger TLBs
   - Integrated L2 cache
   - Faster processor bus
3. Higher Clock Frequency
   - From design
   - From technology
4. Integrate System Components
   - Faster access to memory & I/O
   - Also can reduce cost

# Our Assessment

1. Do More Work per Clock Cycle
   - WinChip 2 already has the high-leverage items
   - Low further improvement for the die size increase

2. Reduce Bus Stalls
   - WinChip 2 already has the high-leverage items
   - Next is integrated L2 cache

   ➔ *Which is too big for the gain*
   *0-20% performance for +55 mm² !*

   ➔ *So we will do 2x L1 cache*
   *Same performance for +20 mm² !*

   ➔ *WinChip 2+*
   *(2x cache)*

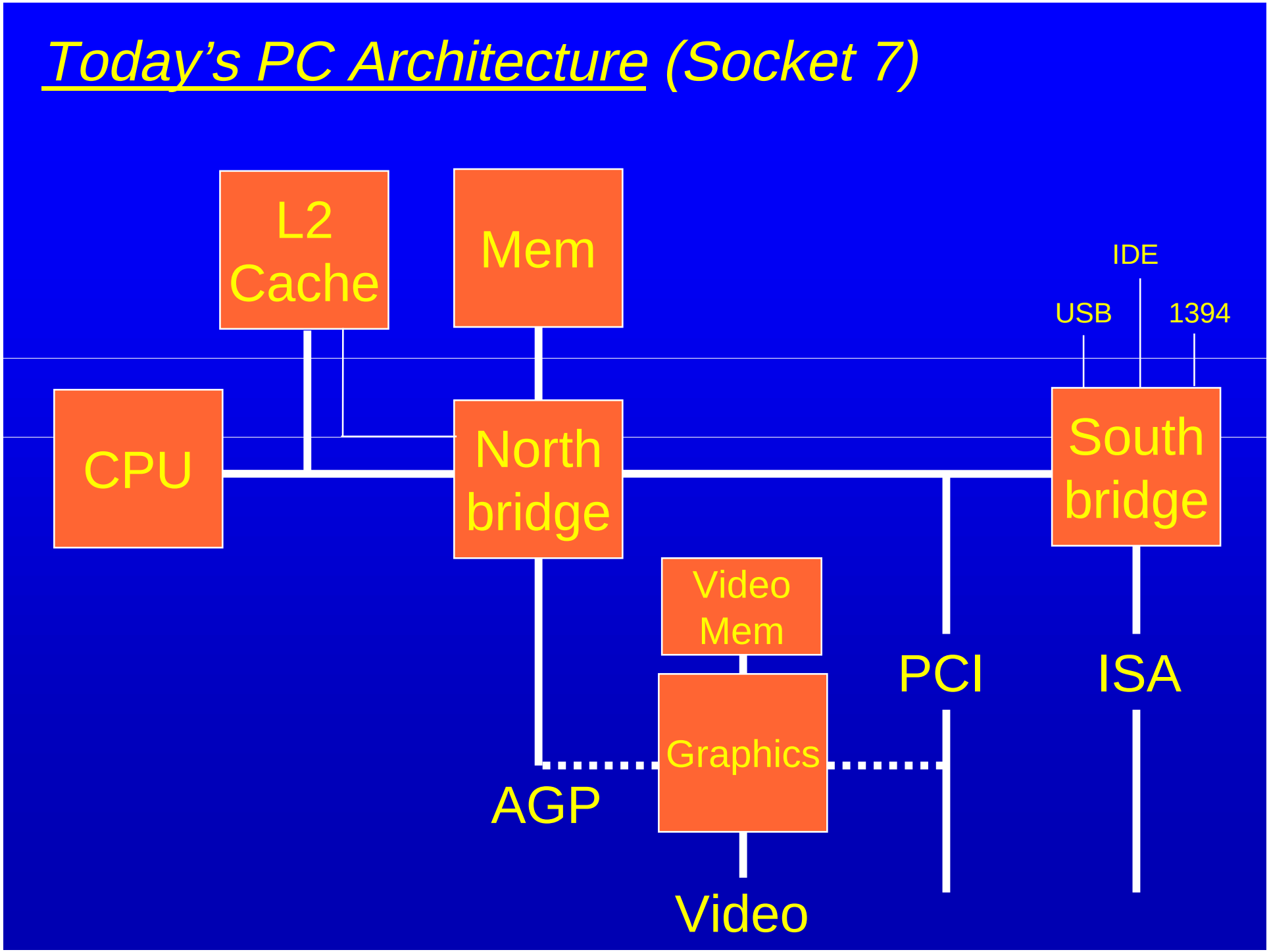
3. Higher Clock Frequency
   - Benefits all applications (but differently)
   - Requires minimal extra die size (cost)

   ➔ *WinChip 3*
   *(2x MHz)*

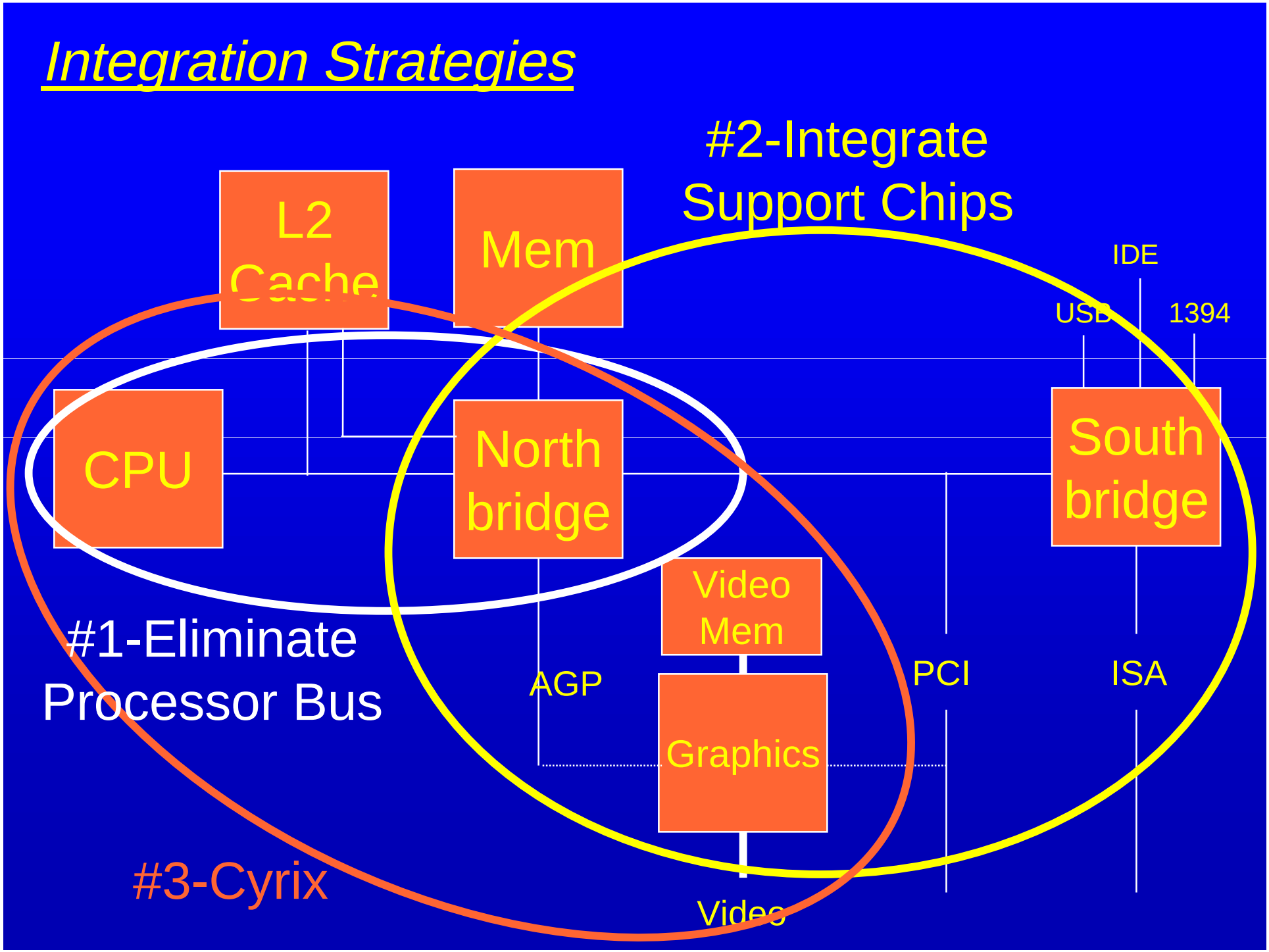
# Bus Wars 2

- Socket 7 vs. Slot 1 (vs. Slot A?)
- Same Driving Force As For ISA vs. MC
  - ➔ *Manufacturer Desire for Exclusivity*
- The Facts For A Low-end PC…
  - Socket 7 is much less expensive
  - And, equally fast (as Slot 1)
  - And, you have a choice of suppliers
- Actually, Any Bus Is A Performance Bottleneck
  - So, we should eliminate the processor bus!
    - ➔ *WinChip 2+NB*

# *Today's PC Architecture (Socket 7)*



# *Integration Strategies*



# Integration Assessment

1. Eliminate Processor Bus
   - + Reduced clocks for processor to get to memory
   - + Reduced cost (2 chips ➔ 1) & board size
   - + Allows processor-graphics mix & match
   - ± ~~New board, but easy (looks like Northbridge chip)~~
   - ± Missing L2 ➔ + internal caches ➔ + performance
2. Integrate Support Chips
   - + Reduces cost & speeds graphics access to memory
   - + Allows graphics–processor mix & match
   - – Still has processor bus bottleneck
3. Cyrix Approach
   - + Reduces cost & speeds access to memory
   - – Ties a processor to a graphics ➔ *no mix & match!*

# Our Strategy

1. Satisfy WinChip 2 Demand
   - Continuing MHz improvements
   - New packages for mobile
   - Improved technology (cost & performance)
   - High volume (multiple fabs & manufacturers)
2. Move To 2x Size Caches = *WinChip 2+*
   - Significant performance gain for modest cost
3. Integrate Processor & Northbridge
   *= WinChip 2+NB (Includes 2x caches)*
4. Double MHz = *WinChip 3*
   - With minimal cost increase (Includes 2x caches)
   - Initially a socket 7 part, then integrated

# IDT WinChip Roadmap