186 Questions & Answers

Q: 80C186:CUSTOMER WANTS TO UPGRADE FROM A 80C186 TO AN 80C186XL, WHAT ARE THE CO-PROCESSORS COMPATABILITY?

A: There is a spec problem on input/out put voltage levels.
The parts do work together. AP-249 addresses these issues
Same is true with 186XL.

Q: 80C186XL:HOW TO CONVERST FROM THE 80C186 TO THE XL DESIGN

A: Faxback doc #2132 Addresses these issues. XL has better
immunity to noise and is on a faster 1 micron technology.
XL is a static core and #2132 has the AC and DC spec
differences, if any.

Q: 80C186XL-CAN YOU PROVIDE THE INDUCTOR/CAPACITOR VALUES FOR THIRD OVERTONE CRYSTAL?

A:THE VALUES LISTED ON PAGE 24-631 ARE TOTALS FOR ALL STRAY CAPACITANCE IN THE CIRCUIT. IN OTHER WORDS, WHEN A 30PF CAP IS SPECIFIED, IT MEANS THAT THE TOTAL CAPACITANCE THAT PIN SHOULD SEE, INCLUDING THE TRACES, THE LEAD FRAME, THE PLATED THRU HOLE, THE WIDTH OF THE TRACE ETC. SHOULD EQUAL 30 PF. GIVE THE STRAY CAP. A VALUE OF ABOUT 3, MAKE THE CAP ABOUT 27. THE SAME GOES FOR THE 3RD OVERTONE XTAL WITH THE FILTER CIRCUIT. YOU CAN MOVE THE VALUES AROUND AS LONG AS YOU MANTAIN THE SAME FILTER CHARACTERISTICS.

Q:80C186-16 - NEED TO KNOW REGARDING THE OSCILLATOR CLOCKIN TIMING SPECS. WHY IS CLKIN RISE TIME SPEC 5NSEC SO TIGHT?
CAN WE USE OSC W/ 7NSEC RISE TIME?

A:MUST ADHERE TO THE 5NSEC SPEC- SEVERAL VENDORS MAKE ACCEPTABLE CANNED OSCILLATORS- FOX, DALE, KRYSTEK AND ARE NOT TO EXPENSIVE (<$5.00/10000 PU).

Q:80C186: IS THERE ANY TEST CODE THAT THE CUSTOMER CAN HAVE

A:No test code exists. Can find start up codes in Faxback
Doc# 3079, 3072. A bunch of various peripheral function
initialization and working example are available on BBS.

For an updated list of BBS Files check BBS CATALOG on FAXBACK.

Q:80C188: DMA CONTROLLER, WHAT IS THE MAX. TRANF. RATE? DOES THE BANDWIDTH CHANGE FOR DIFFERENT MODES OF TRANF AND DOES IT DO CYCLE STEALING.

A: Max transfer rate is 1/4*Fcpu=MBytes/sec for unsynchronized transferes If it is destination synchronized then the bandwidth reduces to 1/5*Fcpu=Mbytes/sec. C186 family of microcontrollers do not provide the cycle stealing DMA feature in the classical sense. The DMA or the CPU will have the full control of the bus at any one time. However you can have interleaved DMA transferes. Once DMA is initiated it takes over the bus after 4 clock cycles, if the CPU is not using the bus and is true for all modes of DMA transfers.