2.0 Embedded Pentium® Processor Electrical Specifications

This section describes the DC and AC specifications for the embedded Pentium processor.

2.1 3.3 V Power Supply

The processor has all V_{CC} 3.3-V inputs. The CLK and PICCLK inputs can tolerate a 5-V input signal. This allows the processor to use 5-V or 3.3-V clock drivers.

2.2 3.3 V Inputs and Outputs

The inputs and outputs of the processor are 3.3 V JEDEC standard levels. Both inputs and outputs are also TTL-compatible, although the inputs cannot tolerate voltage swings above the 3.3 V V_{IN} max. The CLK and PICCLK inputs of the processor are 5 V tolerant. This allows a 5-V clock driver to drive the processor. All other pins are 3.3 V only.

For processor outputs, if the system support components use TTL-compatible inputs, the components will interface to the processor without extra logic. This is because the processor drives according to the 5-V TTL specification (but not beyond 3.3 V).

For processor inputs, the voltage must not exceed the 3.3 V V_{IH3} maximum specification. System support components can consist of 3.3 V devices or open-collector devices. In an open-collector configuration, the external resistor can be biased with the processor's V_{CC}. As the processor's V_{CC} changes from 5 V to 3.3 V, so does this signal's maximum drive.

2.3 Absolute Maximum Ratings

Functional operating conditions are given in the AC and DC specification tables. Functional operation at the maximums is not implied or guaranteed. Extended operation beyond the maximum ratings may affect device reliability. Furthermore, although the Pentium processor contains protective circuitry to resist damage from static electric discharge, always take precautions to avoid high static voltages or electric fields.

Warning: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only.

Table 15. Absolute Maximum Ratings

Parameter	Maximum Rating
Case temperature under bias	–65° C to 110° C
Storage temperature	–65° C to 150° C
3 V Supply voltage with respect to V_{SS}	–0.5 V to +4.6 V
3 V Only Buffer DC Input Voltage	–0.5 V to V_{CC} + 0.5; not to exceed V_{CC3} max[1]
5 V Safe Buffer DC Input Voltage	–0.5 V to 6.5 V[2,3]

NOTES:
1. Applies to all Pentium® processor inputs except CLK and PICCLK.
2. Applies to CLK and PICCLK.
3. See overshoot/undershoot transient specification.

2.4 DC Specifications

Tables 16–18 list the DC specifications that apply to the Pentium processor. The Pentium processor is a 3.3 V part internally. The CLK and PICCLK inputs may be 3.3 V or 5 V inputs. Since the 3.3 V (5 V-safe) input levels defined in Table 16 are the same as the 5 V TTL levels, the CLK and PICCLK inputs are compatible with existing 5 V clock drivers.

Table 16. 3.3 V DC Specifications

T_{CASE} = 0 to 70° C; 3.135 V < V_{CC} < 3.6 V for 100 and 133 MHz devices
T_{CASE} = 0 to 70° C; 3.4 V < V_{CC} < 3.6 V for 166 MHz (VRE device)

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL3}	Input Low Voltage	–0.3	0.8	V	TTL Level, Note 1
V_{IH3}	Input High Voltage	2.0	V_{CC}+0.3	V	TTL Level, Note 1
V_{OL3}	Output Low Voltage		0.4	V	TTL Level, Note 2, Note 1
V_{OH3}	Output High Voltage	2.4		V	TTL Level, Note 3, Note 1
I_{CC3}	Power Supply Current		4250 3400 3250	mA mA mA	166 MHz, Note 4 133 MHz, Note 4 100 MHz, Note 4

NOTES:
1. 3.3 V TTL levels apply to all signals except CLK and PICCLK.
2. Parameter measured at 4 mA.
3. Parameter measured at 3 mA.
4. This value should be used for power supply design. It was determined using a worst-case instruction mix and V_{CC} = 3.6 V. Power supply transient response and decoupling capacitors must be sufficient to handle the instantaneous current changes occurring during transitions from stop clock to full active modes. For more information, refer to “Decoupling Recommendations” on page 22.

Table 17. 3.3 V (5 V-Safe) DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL5}	Input Low Voltage	–0.3	0.8	V	TTL Level†
V_{IH5}	Input High Voltage	2.0	5.55	V	TTL Level†

† Applies to CLK and PICCLK only.

Table 18. Input and Output Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
C_{IN}	Input Capacitance		15	pF	Guaranteed by design.
C_O	Output Capacitance		20	pF	Guaranteed by design.
$C_{I/O}$	I/O Capacitance		25	pF	Guaranteed by design.
C_{CLK}	CLK Input Capacitance		15	pF	Guaranteed by design.
C_{TIN}	Test Input Capacitance		15	pF	Guaranteed by design.
C_{TOUT}	Test Output Capacitance		20	pF	Guaranteed by design.
C_{TCK}	Test Clock Capacitance		15	pF	Guaranteed by design.
I_{LI}	Input Leakage Current				$0 < V_{IN} < V_{CC3}$, This parameter is for input without pullup or pulldown.
I_{LO}	Output Leakage Current				$0 < V_{IN} < V_{CC3}$, This parameter is for input without pullup or pulldown.
I_{IH}	Input Leakage Current		200		V_{IN} = 2.4 V, This parameter is for input with pulldown.
I_{IL}	Input Leakage Current		–400		V_{IN} = 0.4 V, This parameter is for input with pullup.

2.5 AC Specifications

The AC specifications of the Pentium processor consist of setup times, hold times, and valid delays at 0 pF.

2.5.1 Private Bus

When two Pentium processor are operating in dual processor mode, a “private bus” exists to arbitrate for the processor bus and maintain local cache coherency. The private bus consists of two pinout changes:

1. Five pins are added: PBREQ#, PBGNT#, PHIT#, PHITM#, D/P#.
2. Ten output pins become I/O pins: ADS#, D/C#, W/R#, M/IO#, CACHE#, LOCK#, HIT#, HITM#, HLDA, SCYC.

The new pins are given AC specifications of valid delays at 0 pF, setup times, and hold times. Simulate with these parameters and their respective I/O buffer models to guarantee that proper timings are met.

The AC specification gives input setup and hold times for the ten signals that become I/O pins. These setup and hold times must only be met when a dual processor is present in the system.

2.5.2 Power and Ground

For clean on-chip power distribution, the Pentium processor has 53 V_{CC} (power) and 53 V_{SS} (ground) inputs. Power and ground connections must be made to all external V_{CC} and V_{SS} pins of the processor. On the circuit board all V_{CC} pins must be connected to a V_{CC} plane. All V_{SS} pins must be connected to a V_{SS} plane.

2.5.3 Decoupling Recommendations

Liberal decoupling capacitance should be placed near the processor. Transient power surges can occur when the processor is driving its address and data buses at high frequencies. This is most common when driving large capacitive loads.

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance can be reduced by minimizing the length of the circuit board traces between the processor and the decoupling capacitors.

These capacitors should be evenly distributed around each component on the 3.3 V plane. Capacitor values should be chosen to ensure that they eliminate both low and high frequency noise components.

For the Pentium processor, the power consumption can transition from a low power level to a much higher level (or high-to-low power) very rapidly. A typical example is when entering or exiting the Stop Grant state. Other examples are when executing a HALT instruction (causing the processor to enter the Auto HALT Powerdown state) or when transitioning from HALT to the Normal state. All these examples may cause abrupt changes in the power being consumed by the processor. Note that the Auto HALT Powerdown feature is always enabled even when other power management features are not implemented.

Bulk storage capacitors with a low ESR (Effective Series Resistance) in the 10 to 100 µF range are required to maintain a regulated supply voltage during the interval between the time the current load changes and the point at which the regulated power supply output reacts to the change in load. In order to reduce the ESR, it may be necessary to place several bulk storage capacitors in parallel.

These capacitors should be placed near the processor (on the 3.3 V plane) to ensure that the supply voltage stays within specified limits during changes in the supply current during operation.

2.5.4 Connection Specifications

All NC and INC pins must remain unconnected. For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to V_{CC}. Unused active high inputs should be connected to ground.

2.5.5 AC Timing Tables

The AC specifications given in Table 19 and Table 20 consist of output delays, input setup requirements and input hold requirements for a 66-MHz external bus. All AC specifications (with the exception of those for the TAP signals and APIC signals) are relative to the rising edge of the CLK input.

All timings are referenced to 1.5 V for both “0” and “1” logic levels unless otherwise specified. Within the sampling window, a synchronous input must be stable for correct processor operation. Each valid delay is specified for a 0 pF load. The system designer should use I/O buffer models to account for signal flight time delays.

The following applies to all standard TTL signals used with the Pentium processor family:

- TTL input test waveforms are assumed to be 0 to 3 V transitions with 1 V/ns rise and fall times.
- 0.3 V/ns ≤ input rise/fall time ≤ 5 V/ns.

Table 19. AC Specifications

T_{CASE} = 0 to 70° C; 3.135 V < V_{CC} < 3.6 V for 100 and 133 MHz devices, C_L = 0 pF
T_{CASE} = 0 to 70° C; 3.4 V < V_{CC} < 3.6 V for 166 MHz (VRE device), C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	33.33	66.6	MHz		
t_{1a}	CLK Period	15.0	30.0	ns	5	
t_{1b}	CLK Period Stability			ps		Adjacent Clocks, Notes 1, 21
t_2	CLK High Time	4.0		ns	5	2 V, Note 1
t_3	CLK Low Time	4.0		ns	5	0.8 V, Note 1
t_4	CLK Fall Time	0.15	1.5	ns	6	2.0 V–0.8 V, Note 1
t_5	CLK Rise Time	0.15	1.5	ns	5	0.8 V–2.0 V, Note 1
t_{6a}	PWT, PCD, CACHE# Valid Delay	1.0	7.0	ns	6	
t_{6b}	AP Valid Delay	1.0	8.5	ns	6	
t_{6c}	BE7#–BE0#, LOCK# Valid Delay	0.9	7.0	ns	6	
t_{6d}	ADS# Valid Delay	0.8	6.0	ns	6	
t_{6e}	ADSC#, D/C#, W/R#, SCYC, Valid Delay	0.8	7.0	ns	6	
t_{6f}	M/IO# Valid Delay	0.8	5.9	ns	6	
t_{6g}	A16–A3 Valid Delay	0.5	6.3	ns	6	
t_{6h}	A31–A17 Valid Delay	0.6	6.3	ns	6	
t_7	ADS#, ADSC#, AP, A31–A3, PWT, PCD, BE7#–BE0#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	ns	7	1
t_{8a}	APCHK#, IERR#, FERR# Valid Delay	1.0	8.3	ns	6	3
t_{8b}	PCHK# Valid Delay	1.0	7.0	ns	6	3
t_{9a}	BREQ Valid Delay	1.0	8.0	ns	6	3
t_{9b}	SMIACT# Valid Delay	1.0	7.3	ns	6	3
t_{9c}	HLDA Valid Delay	1.0	6.8	ns	6	
t_{10a}	HIT# Valid Delay	1.0	6.8	ns	6	
t_{10b}	HITM# Valid Delay	0.7	6.0	ns	6	
t_{11a}	PM1–PM0, BP3–BP0 Valid Delay	1.0	10.0	ns	6	
t_{11b}	PRDY Valid Delay	1.0	8.0	ns	6	
t_{12}	D63–D0, DP7–DP0 Write Data Valid Delay	1.3	7.5	ns	6	
t_{13}	D63–D0, DP3–DP0 Write Data Float Delay		10.0	ns	7	1
t_{14}	A31–A5 Setup Time	6.0		ns	8	22
t_{15}	A31–A5 Hold Time	1.0		ns	8	
t_{16a}	INV, AP Setup Time	5.0		ns	8	
t_{16b}	EADS# Setup Time	5.0		ns	8	
t_{17}	EADS#, INV, AP Hold Time	1.0		ns	8	
t_{18a}	KEN# Setup Time	5.0		ns	8	

NOTE: See Table 21 for notes.

Table 19. AC Specifications

T_{CASE} = 0 to 70° C; 3.135 V < V_{CC} < 3.6 V for 100 and 133 MHz devices, C_L = 0 pF
T_{CASE} = 0 to 70° C; 3.4 V < V_{CC} < 3.6 V for 166 MHz (VRE device), C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{18b}	NA#, WB/WT# Setup Time	4.5		ns	8	
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.0		ns	8	
t_{20}	BRDY#, BRDYC# Setup Time	5.0		ns	8	
t_{21}	BRDY#, BRDYC# Hold Time	1.0		ns	8	
t_{22}	AHOLD, BOFF# Setup Time	5.5		ns	8	
t_{23}	AHOLD, BOFF# Hold Time	1.0		ns	8	
t_{24a}	BUSCHK#, EWBE#, HOLD Setup Time	5.0		ns	8	
t_{24b}	PEN# Setup Time	4.8		ns	8	
t_{25a}	BUSCHK#, EWBE#, PEN# Hold Time	1.0		ns	8	
t_{25b}	HOLD Hold Time	1.5		ns	8	
t_{26}	A20M#, INTR, STPCLK# Setup Time	5.0		ns	8	9, 12
t_{27}	A20M#, INTR, STPCLK# Hold Time	1.0		ns	8	10
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.0		ns	8	9, 12, 13
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.0		ns	8	10
t_{30}	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2.0		CLKs		11, 13
t_{31}	R/S# Setup Time	5.0		ns	8	9, 12, 13
t_{32}	R/S# Hold Time	1.0		ns	8	10
t_{33}	R/S# Pulse Width, Async.	2.0		CLKs		11, 13
t_{34}	D63–D0, DP7–DP0 Read Data Setup Time	2.8		ns	8	
t_{35}	D63–D0, DP7–DP0 Read Data Hold Time	1.5		ns	8	
t_{36}	RESET Setup Time	5.0		ns	9	8, 9, 12
t_{37}	RESET Hold Time	1.0		ns	9	8, 10
t_{38}	RESET Pulse Width, V_{CC} & CLK Stable	15.0		CLKs	9	8, 13
t_{39}	RESET Active After V_{CC} & CLK Stable	1.0		ms	9	Power up
t_{40}	Reset Configuration Signals (INIT, FLUSH#, FRCMC#) Setup Time	5.0		ns	9	9, 12, 13
t_{41}	Reset Configuration Signals (INIT, FLUSH#, FRCMC#) Hold Time	1.0		ns	9	10
t_{42a}	Reset Configuration Signals (INIT, FLUSH#, FRCMC#) Setup Time, Async.	2.0		CLKs	9	To RESET falling edge, Note 12
t_{42b}	Reset Configuration Signals (INIT, FLUSH#, FRCMC#, BRDYC#, BUSCHK#) Hold Time, Async.	2.0		CLKs	9	To RESET falling edge, Note 23
t_{42d}	Reset Configuration Signal BRDYC# Hold Time, RESET driven synchronously	1.0		ns		To RESET falling edge, 1, 23
t_{43a}	BF, CPUTYP Setup Time	1.0		ms	9	To RESET falling edge, Note 18

NOTE: See Table 21 for notes.

Table 19. AC Specifications

T_{CASE} = 0 to 70° C; 3.135 V < V_{CC} < 3.6 V for 100 and 133 MHz devices, C_L = 0 pF
T_{CASE} = 0 to 70° C; 3.4 V < V_{CC} < 3.6 V for 166 MHz (VRE device), C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{43b}	BF, CPUTYP Hold Time	2.0		CLKs	9	To RESET falling edge, Note 18
t_{43c}	APICEN, BE4# Setup Time	2.0		CLKs	9	To RESET falling edge
t_{43d}	APICEN, BE4# Hold Time	2.0		CLKs	9	To RESET falling edge
t_{44}	TCK Frequency		16.0	MHz		
t_{45}	TCK Period	62.5		ns	5	
t_{46}	TCK High Time	25.0		ns	5	2 V, Note 1
t_{47}	TCK Low Time	25.0		ns	5	0.8 V, Note 1
t_{48}	TCK Fall Time		5.0	ns	5	2.0 V–0.8 V, Notes 1,5,6
t_{49}	TCK Rise Time		5.0	ns	5	0.8 V–2.0 V, Notes 1,5,6
t_{50}	TRST# Pulse Width	40.0		ns	11	Asynchronous, Note 1
t_{51}	TDI, TMS Setup Time	5.0		ns	10	4
t_{52}	TDI, TMS Hold Time	13.0		ns	10	4
t_{53}	TDO Valid Delay	3.0	20.0	ns	10	5
t_{54}	TDO Float Delay		25.0	ns	10	1, 5
t_{55}	All Non-Test Outputs Valid Delay	3.0	20.0	ns	10	2, 5, 7
t_{56}	All Non-Test Outputs Float Delay		25.0	ns	10	1, 2, 5, 7
t_{57}	All Non-Test Inputs Setup Time	5.0		ns	10	2, 4, 7
t_{58}	All Non-Test Inputs Hold Time	13.0		ns	10	2, 4, 7
APIC AC Specifications						
t_{60a}	PICCLK Frequency	2.0	16.66	MHz		
t_{60b}	PICCLK Period	60.0	500.0	ns	5	
t_{60c}	PICCLK High Time	15.0		ns	5	
t_{60d}	PICCLK Low Time	15.0		ns	5	
t_{60e}	PICCLK Rise Time	0.15	2.5	ns	5	
t_{60f}	PICCLK Fall Time	0.15	2.5	ns	5	
t_{60g}	PICD1–PICD0 Setup Time	3.0		ns	8	To PICCLK
t_{60h}	PICD1–PICD0 Hold Time	2.5		ns	8	To PICCLK
t_{60i}	PICD1–PICD0 Valid Delay (LtoH)	4.0	38.0	ns	6	From PICCLK, Notes 24, 25
t_{60j}	PICD1–PICD0 Valid Delay (HtoL)	4.0	22.0	ns	6	From PICCLK, Notes 24, 25
t_{61}	PICCLK Setup Time	5.0		ns		To CLK, Note 26
t_{62}	PICCLK Hold Time	2.0		ns		To CLK, Note 26
t_{63}	PICCLK Ratio (CLK/PICCLK)	4				27

NOTE: See Table 21 for notes.

Table 20. Dual Processor Mode AC Specifications

T_{CASE} = 0 to 70° C; 3.135 V < V_{CC} < 3.6 V for 100 and 133 MHz devices, C_L = 0 pF
T_{CASE} = 0 to 70° C; 3.4 V < V_{CC} < 3.6 V for 166 MHz (VRE device), C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{80a}	PBREQ#, PBGNT#, PHIT# Flight Time	0	2.0	ns		20, 25
t_{80b}	PHITM# Flight Time	0	1.8	ns		20, 25
t_{83a}	A31–A5 Setup Time	3.7		ns	8	14, 17, 22
t_{83b}	D/C#, W/R#, CACHE#, LOCK#, SCYC Setup Time					
t_{83c}	ADS#, M/IO# Setup Time	5.8		ns	8	14, 17
t_{83d}	HIT#, HITM# Setup Time	6.0		ns	8	14, 17
t_{83e}	HLDA Setup Time	6.0		ns	8	14, 17
t_{84}	ADS#, D/C#, W/R#, M/IO#, CACHE#, LOCK#, A31–A5, HLDA, HIT#, HITM#, SCYC Hold Time	1.0		ns	8	14, 17
t_{85}	DPEN# Valid Time		10.0	CLKs		14, 15, 19
t_{86}	DPEN# Hold Time	2.0		CLKs		14, 16, 19
t_{87}	APIC ID (BE3#–BE0#) Setup Time	2.0		CLKs	9	To RESET falling edge, Note 19
t_{88}	APIC ID (BE3#–BE0#) Hold Time	2.0		CLKs	9	From RESET falling edge, Note 19
t_{89}	D/P# Valid Delay	1.0	8.0	ns	6	Primary Processor Only

NOTE: See Table 21 for table notes.

Table 21. Notes for Tables 19 and 20

1. Not 100% tested. Guaranteed by design/characterization.
2. Non-test outputs and inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to boundary scan operations.
3. APCHK#, FERR#, HLDA, IERR#, LOCK#, and PCHK# are glitch-free outputs. Glitch-free signals monotonically transition without false transitions.
4. Referenced to TCK rising edge.
5. Referenced to TCK falling edge.
6. 1 ns can be added to the maximum TCK rise and fall times for every 10 MHz of frequency below 33 MHz.
7. During probe mode operation, do not use the boundary scan timings ($t_{55\text{-}58}$).
8. FRCMC# should be tied to V_{CC} (high) to ensure proper operation of the Pentium processor as a primary processor.
9. Setup time is required to guarantee recognition on a specific clock. The Pentium processor must meet this specification for dual processor operation for the FLUSH# and RESET signals.
10. Hold time is required to guarantee recognition on a specific clock. The Pentium processor must meet this specification for dual processor operation for the FLUSH# and RESET signals.
11. To guarantee proper asynchronous recognition, the signal must have been deasserted (inactive) for a minimum of two clocks before being returned active and must meet the minimum pulse width.
12. This input may be driven asynchronously. However, when operating two processors in dual processing mode, FLUSH# and RESET must be asserted synchronously to both processors.
13. When driven asynchronously, RESET, NMI, FLUSH#, R/S#, INIT, and SMI# must be deasserted (inactive) for a minimum of two clocks before being returned active.
14. Timings are valid only when dual processor is present.
15. Maximum time DPEN# is valid from rising edge of RESET.
16. Minimum time DPEN# is valid after falling edge of RESET.
17. The D/C#, M/IO#, W/R#, CACHE#, and A31–A5 signals are sampled only on the CLK during which ADS# is active.
18. BF and CPUTYP should be strapped to V_{CC} or V_{SS}.
19. RESET is synchronous in dual processing mode and functional redundancy checking mode. All signals that have a setup or hold time with respect to a falling or rising edge of RESET in UP mode should be measured with respect to the first processor clock edge in which RESET is sampled either active or inactive in dual processing and functional redundancy checking modes.
20. The PHIT# and PHITM# signals operate at the core frequency.
21. These signals are measured on the rising edge of adjacent CLKs at 1.5 V. To ensure a 1:1 relationship between the amplitude of the input jitter and the internal and external clocks, the jitter frequency spectrum should not have any power spectrum peaking between 500 KHz and 1/3 of the CLK operating frequency. The amount of jitter present must be accounted for as a component of CLK skew between devices.
22. In dual processing mode, timing t_{14} is replaced by t_{83a}. Timing t_{14} is required for external snooping (e.g., address setup to the CLK in which EADS# is sampled active) in both uniprocessor and dual processor modes.
23. BRDYC# and BUSCHK# are used as reset configuration signals to select buffer size.
24. This assumes an external pullup resistor to V_{CC} and a lumped capacitive load. The pullup resistor must be between 300 Ohms and 1 KOhms, the capacitance must be between 20 pF and 120 pF, and the RC product must be between 3 ns and 36 ns. V_{OL} for PICD1–PICD0 is 0.55 V.
25. This is a flight time specification that includes both flight time and clock skew. The flight time is the time from when the unloaded driver crosses 1.5 V (50% of min. V_{CC}), to when the receiver crosses the 1.5 V level (50% of min. V_{CC}). See Figure 12.
26. This is for the lock-step operation of the component only. This guarantees that APIC interrupts will be recognized on specific clocks to support two processors running in a lock step fashion, including FRC mode. FRC on the APIC pins is not supported but mismatches on these pins will result in a mismatch on other pins of the CPU.
27. The CLK to PICCLK ratio for lock-step operation must be an integer and the ratio (CLK/PICCLK) cannot be smaller than 4:1.

Figure 5. Clock Waveform

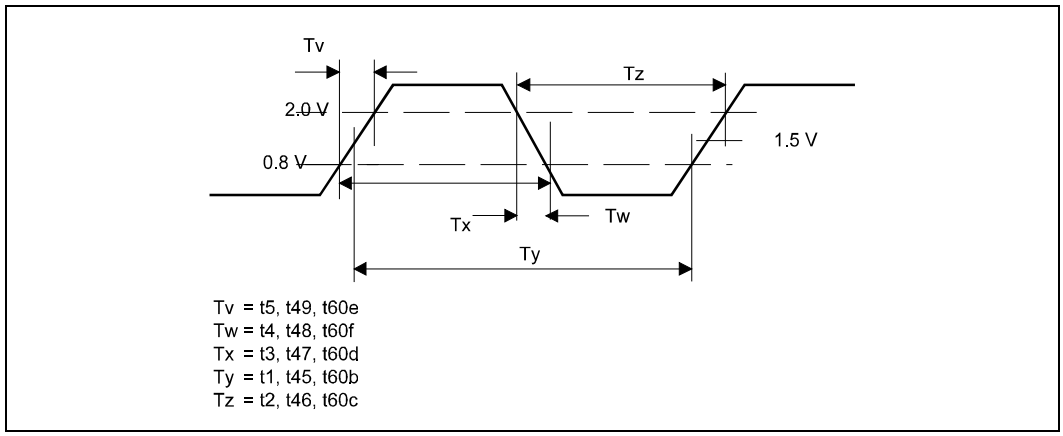


Figure 6. Valid Delay Timings

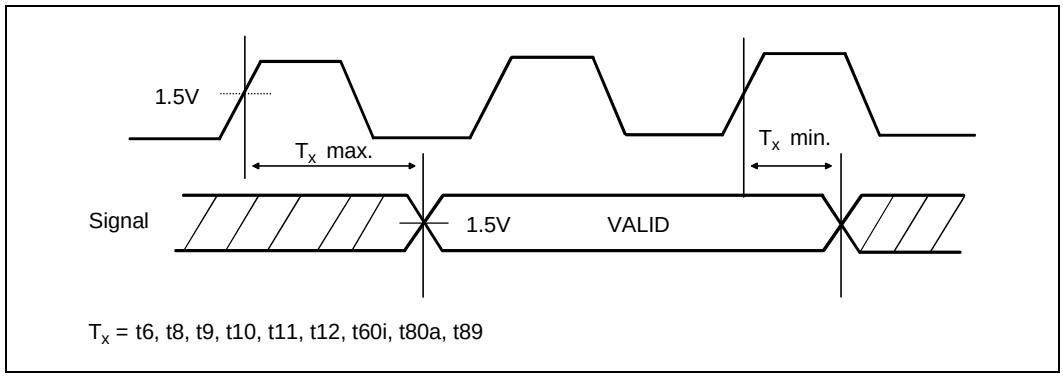


Figure 7. Float Delay Timings

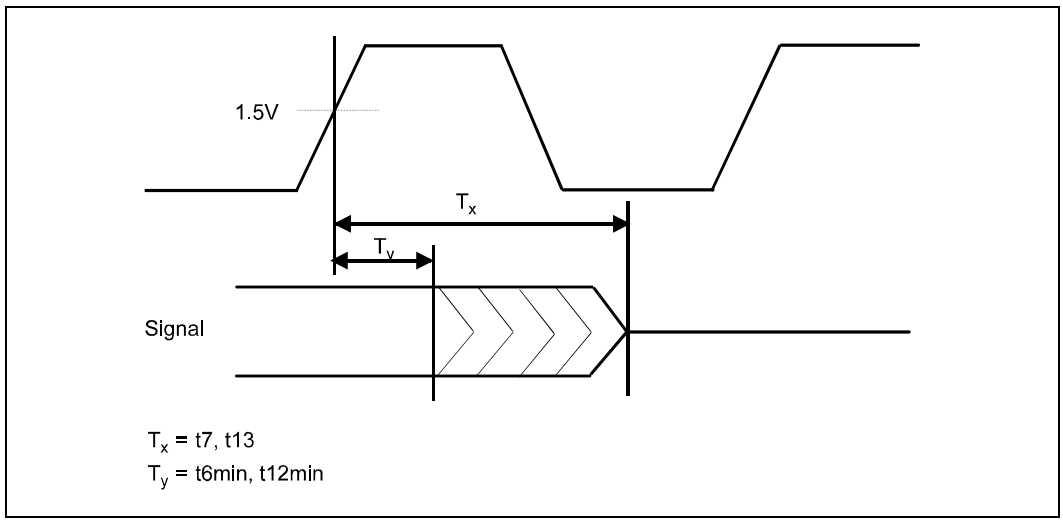
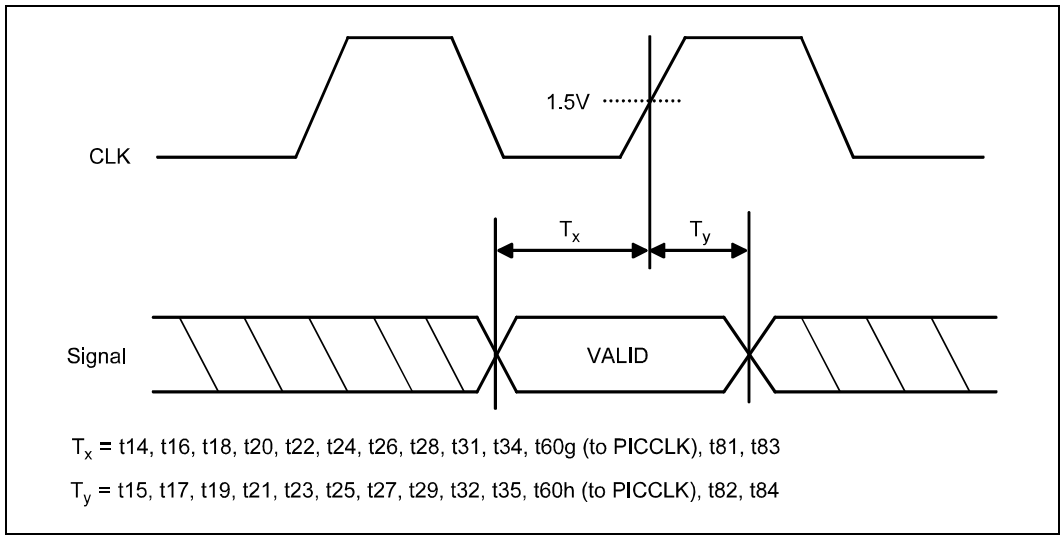


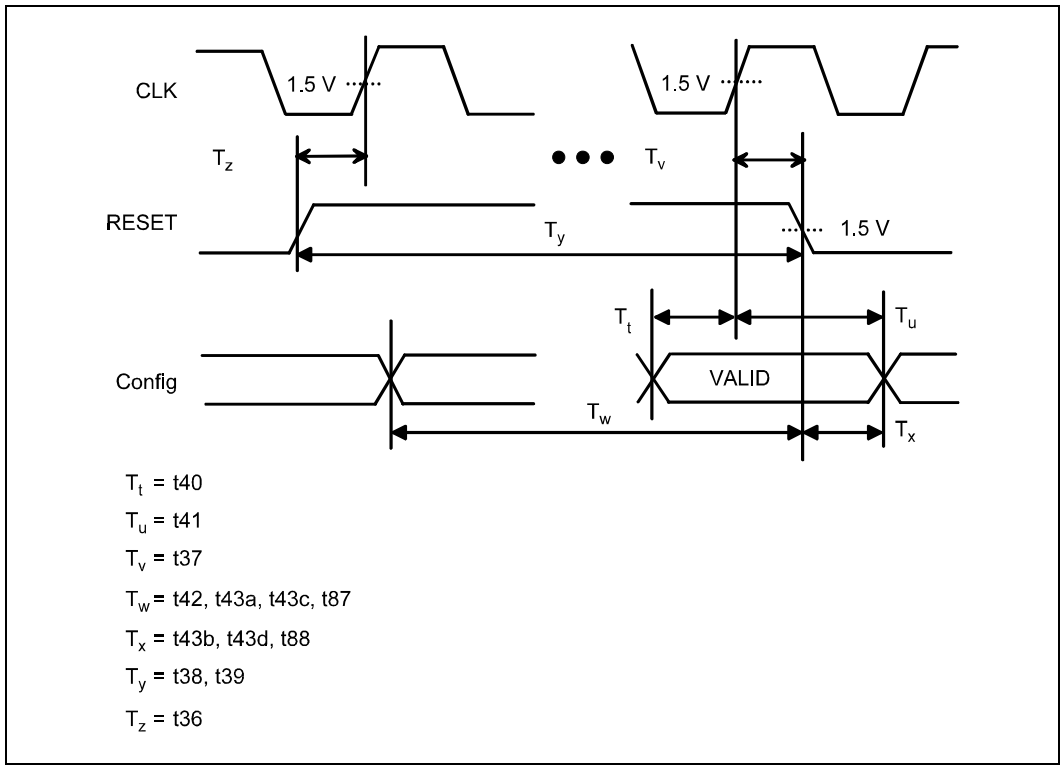
Figure 8. Setup and Hold Timings



T_x = t14, t16, t18, t20, t22, t24, t26, t28, t31, t34, t60g (to PICCLK), t81, t83

T_y = t15, t17, t19, t21, t23, t25, t27, t29, t32, t35, t60h (to PICCLK), t82, t84

Figure 9. Reset and Configuration Timings



T_t = t40

T_u = t41

T_v = t37

T_w = t42, t43a, t43c, t87

T_x = t43b, t43d, t88

T_y = t38, t39

T_z = t36

Figure 10. Test Timings

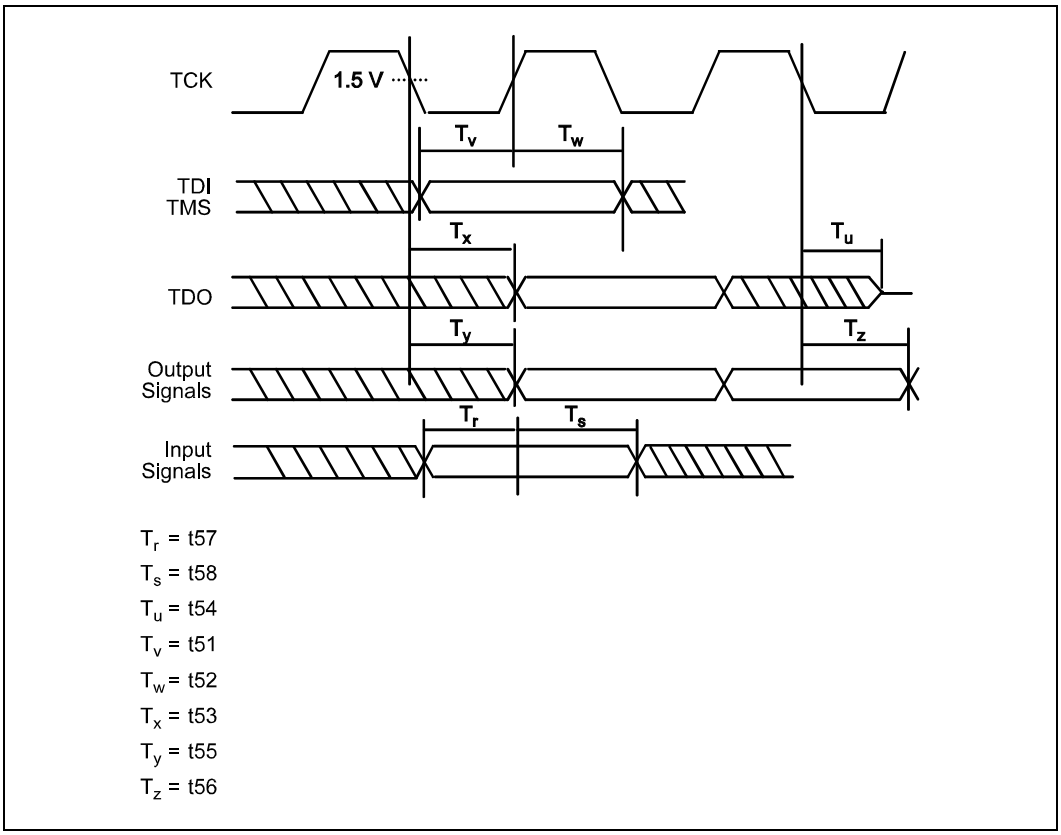


Figure 11. Test Reset Timings

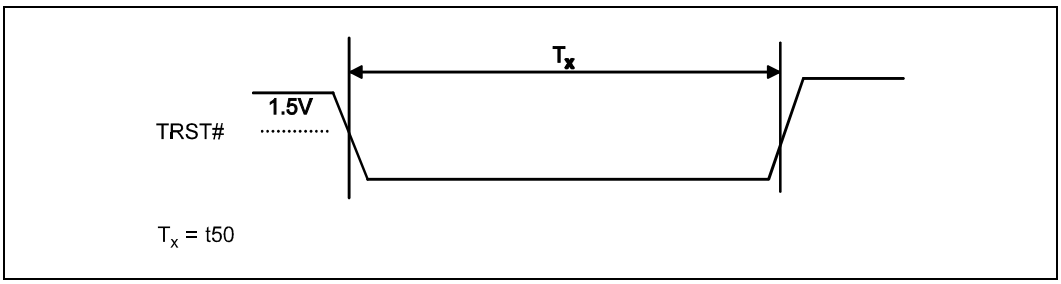


Figure 12. 50% V_{CC} Measurement of Flight Time