9.0 Pentium Processor® with MMX™ Technology Electrical Specifications

This section describes the electrical differences between the Pentium processor with MMX technology and the Pentium processor, and the AC and DC specifications of the Pentium processor with MMX technology.

9.1 Electrical Characteristics

When creating a Pentium processor with MMX technology design based on an existing Pentium processor design, there are a number of electrical differences that require attention. The following sections highlight key electrical issues pertaining to the Pentium processor with MMX technology power supplies, connection specifications and buffer models.

Note that it is possible to design a single motherboard that supports more than one member of the Pentium processor family. Refer to *Pentium® Processor Flexible Motherboard Design Guidelines* (order number 243187) for more information and specific implementation examples.

9.1.1 Power Supplies

The main electrical difference between the Pentium processor with MMX technology and the Pentium processor is the operating voltage. The Pentium processor with MMX technology requires two separate voltage inputs, V_{CC2} and V_{CC3}. The V_{CC2} pins supply power to the Pentium processor with MMX technology core, while the V_{CC3} pins supply power to the processor I/O pins.

The Pentium processor, on the other hand, requires a single voltage supply for all V_{CC} pins. This single supply powers both the core and I/O pins of the Pentium processor.

By connecting all the V_{CC2} pins together and all the V_{CC3} pins together on separate power islands, Pentium processor designs can easily be converted to support the Pentium processor with MMX technology. In order to maintain compatibility with Pentium processor-based platforms, the Pentium processor with MMX technology supports the standard 3.3-V specification on its V_{CC3} pins.

9.1.2 Power Supply Sequencing

There is no specific power sequence required for powering up or powering down the separate V_{CC2} and V_{CC3} supplies of the Pentium processor with MMX technology. It is recommended that the V_{CC2} and V_{CC3} supplies be turned on or off within one second of each other.

9.1.3 Connection Specifications

Connection specifications for the power and ground inputs, 3.3-V inputs and outputs, and the NC/INC and unused inputs are discussed in the following sections.

9.1.3.1 Power and Ground

For clean on-chip power distribution, the embedded Pentium processor with MMX technology has 28 V_{CC3} (I/O power), 25 V_{CC2} (core power) and 53 V_{SS} (ground) inputs. Power and ground connections must be made to all external V_{CC} and V_{SS} pins of the Pentium processor with MMX technology. On the circuit board, all V_{CC3} pins must be connected to a 3.3-V V_{CC} plane. All V_{CC3} pins must be connected to a 2.8-V V_{CC} plane. All V_{SS} pins must be connected to a V_{SS} plane.

9.1.3.2 V_{CC2} and V_{CC3} Measurement Specification

The values of V_{CC2} and V_{CC3} should be measured at the bottom side of the processor pins using an oscilloscope with a 3 dB bandwidth of at least 20 MHz (100 MS/s digital sampling rate). There should be a short isolation ground lead attached to a processor pin on the bottom side of the board.

The measurement should be taken at the following V_{CC}/V_{SS} pairs: AN13/AM10, AN21/AM18, AN29/ AM26, AC37/Z36, U37/R36, L37/H36, A25/B28, A17/B20, A7/B10, G1/K2, S1/V2, AC1/Z2. One-half of these pins are V_{CC2} while the others are V_{CC3}; the operating ranges for the V_{CC2} and V_{CC3} pins are specified at different voltages. See Table 61 for the specification.

The display should show continuous sampling of the voltage line, at 20 mV/div, and 500 ns/div with the trigger point set to the center point of the range. Slowly move the trigger to the high and low ends of the specification, and verify that excursions beyond these limits are not observed. There are no allowances for crossing the high and low limits of the voltage specification. For more information on measurement techniques, see *Voltage Guidelines for Pentium® Processors with MMX™ Technology* (order number 243186).

9.1.3.3 Decoupling Recommendations

Liberal decoupling capacitance should be placed near the Pentium processor with MMX technology. The Pentium processor with MMX technology, when driving its large address and data buses at high frequencies, can cause transient power surges, particularly when driving large capacitive loads.

Low inductance capacitors and interconnects are recommended for best high-frequency electrical performance. Inductance can be reduced by shortening circuit board traces between the Pentium processor with MMX technology and decoupling capacitors as much as possible. These capacitors should be evenly distributed around each component on the power plane. Capacitor values should be chosen to ensure they eliminate both low and high frequency noise components.

For the Pentium processor with MMX technology, the power consumption can transition from a low level of power to a much higher level (or high to low power) very rapidly. A typical example would be entering or exiting the Stop Grant State. Another example would be executing a HALT instruction, causing the Pentium processor with MMX technology to enter the AutoHALT Power Down State, or transitioning from HALT to the Normal State. All of these examples may cause abrupt changes in the power being consumed by the Pentium processor with MMX technology. Note that the AutoHALT Power Down feature is always enabled even when other power management features are not implemented.

Bulk storage capacitors with a low Effective Series Resistance (ESR) in the 10-Ω to 100-Ω range are required to maintain a regulated supply voltage during the interval between the time the current load changes and the point that the regulated power supply output can react to the change in load. In order to reduce the ESR, it may be necessary to place several bulk storage capacitors in parallel.

These capacitors should be placed near the Pentium processor with MMX technology on both the V_{CC2} and V_{CC3} plane to ensure that the supply voltage stays within specified limits during changes in the supply current during operation.

Detailed decoupling recommendations are provided in *Flexible Motherboard Design Guidelines* (order number 243187).

Note: Reducing available bulk capacitance could degrade long term system reliability.

9.1.3.4 3.3-V Inputs and Outputs

The inputs and outputs of the Pentium processor with MMX technology comply with the 3.3-V JEDEC standard levels. Both inputs and outputs are also TTL-compatible, although the inputs cannot tolerate voltage swings above the V_{IN3} (max) specification.

System support components which use TTL-compatible inputs will interface to the Pentium processor with MMX technology without extra logic. This is because the Pentium processor drives according to the 5-V TTL specification (but not beyond 3.3 V).

For Pentium processor with MMX technology inputs, the voltage must not exceed the 3.3-V V_{IN3} (max) specification. System support components can consist of 3.3-V devices or open-collector devices. In an open-collector configuration, the external resistor should be biased to V_{CC3}.

All pins, including the CLK and PICCLK of the Pentium processor with MMX technology, are 3.3 V-tolerant-only. When an 8259A interrupt controller is used, for example, the system must provide level converters between the 8259A and the Pentium processor with MMX technology.

9.1.3.5 NC/INC and Unused Inputs

Important: All NC and INC pins must remain unconnected.

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to V_{CC3}. Unused active high inputs should be connected to V_{SS} (ground).

9.1.3.6 Private Bus

When two Pentium processors with MMX technology are operating in dual processor mode, a “private bus” exists to arbitrate for the processor bus and maintain local cache coherency. The private bus consists of two pinout changes:

- Five pins are added: PBREQ#, PBGNT#, PHIT#, PHITM#, D/P#.
- Ten output pins become I/O pins: ADS#, D/C#, W/R#, M/IO#, CACHE#, LOCK#, HIT#, HITM#, HLDA, SCYC, BE4#.

The new pins are given AC specifications of valid delays at 0 pF, setup times and hold times. Simulate with these parameters and their respective I/O buffer models to guarantee that proper timings are met.

The AC specification gives input setup and hold times for the ten signals that become I/O pins. These setup and hold times must be met only when a dual processor is present in the system.

9.1.4 Buffer Models

The structure of the buffer models for the Pentium processor with MMX technology and the Pentium processor are identical. Some of the values of the components have changed to reflect the minor manufacturing process and package differences between the processors. The system should see insignificant differences between the AC behavior of the Pentium processor with MMX technology and the Pentium processor.

Simulation of AC timings using the Pentium processor with MMX technology buffer models is recommended to ensure robust system designs. Pay specific attention to the signal quality restrictions imposed by 3.3-V buffers.

9.2 Absolute Maximum Ratings

Table 60 provides stress ratings only. Functional operation at the Absolute Maximum Ratings is not implied or guaranteed. Functional operating conditions are given in the AC and DC specification tables.

Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the Pentium processor with MMX technology contains protective circuitry to resist damage from electrostatic discharge, always take precautions to avoid high static voltages or electric fields.

Table 60. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
	Storage Temperature	–65	150	°C
	Case Temperature Under Bias	–65	110	°C
V_{CC3}	V_{CC3} Supply Voltage with respect to V_{SS}	–0.5	4.6	V
V_{CC2}	V_{CC2} Supply Voltage with respect to V_{SS}	–0.5	3.7	V
V_{IN3}	3-V Only Buffer DC Input Voltage	–0.5	V_{CC3} +0.5 (not to exceed V_{CC3} max)	V

Warning: Stressing the device beyond the Absolute Maximum Ratings may cause permanent damage. These are stress ratings only. Operation beyond the DC specifications is not recommended or guaranteed and extended exposure beyond the DC specifications may affect device reliability.

9.3 DC Specifications

Tables 61 through 64 list the DC specifications for the Pentium processor with MMX technology.

Table 61. V_{CC} and T_{CASE} Specifications

Symbol	Parameter	Min	Nom.	Max	Unit	Notes
T_{CASE}	Case Temperature	0		70	°C	
V_{CC2}	V_{CC2} Voltage	2.7	2.8	2.9	V	Range = 2.8 ± 3.57%†
V_{CC3}	V_{CC3} Voltage	3.135	3.3	3.6	V	Range = 3.3 –5%, +9.09%†

† See "V_{CC2} and V_{CC3} Measurement Specification" on page 22.

Table 62. 3.3 V DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL3}	Input Low Voltage	–0.3	0.8	V	TTL Level
V_{IH3}	Input High Voltage	2.0	V_{CC3} +0.3	V	TTL Level (1)
V_{OL3}	Output Low Voltage		0.4	V	TTL Level (2, 3)
V_{OH3}	Output High Voltage	2.4		V	TTL Level (4)

NOTES:
1. Parameter measured at nominal V_{CC3} which is 3.3 V.
2. Parameter measured at –4 mA.
3. In dual processing systems, up to a 10 mA load from the second processor may be observed on the PCHK# signal. Based on silicon characterization data, V_{OL3} of PCHK# will remain less than 400 mV even with a 10 mA load. PCHK# V_{OL3} will increase to approximately 500 mV with a 14 mA load (worst case for a DP system with a 4 mA system load).
4. Parameter measured at 3 mA.

Table 63. ICC Specifications

Measured at V_{CC2}=2.9 V and V_{CC3}=3.6 V

Symbol	Parameter	Min	Max	Unit	Notes
I_{CC2}	Power Supply Current		6500 5700	mA mA	233 MHz 200 MHz†
I_{CC3}	Power Supply Current		750 650	mA mA	233 MHz 200 MHz†

† This value should be used for power supply design. It was determined using a worst case instruction mix and maximum V_{CC}. Power supply transient response and decoupling capacitors must be sufficient to handle the instantaneous current changes occurring during transitions from Stop Clock to full Active modes.

Table 64. Input and Output Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
C_{IN}	Input Capacitance		15	pF	Guaranteed by design
C_O	Output Capacitance		20	pF	Guaranteed by design
$C_{I/O}$	I/O Capacitance		25	pF	Guaranteed by design
C_{CLK}	CLK Input Capacitance		15	pF	Guaranteed by design
C_{TIN}	Test Input Capacitance		15	pF	Guaranteed by design
C_{TOUT}	Test Output Capacitance		20	pF	Guaranteed by design
C_{TCK}	Test Clock Capacitance		15	pF	Guaranteed by design
I_{LI}	Input Leakage Current		±15	µA	$0 < V_{IN} < V_{IL}$, $V_{IH} > V_{IN} > V_{CC}$, Note 1
I_{LO}	Output Leakage Current		±15	µA	$0 < V_{IN} < V_{IL}$, $V_{IH} > V_{IN} > V_{CC}$, Note 1
I_{IH}	Input Leakage Current		200	µA	V_{IN} = 2.4 V, Note 2
I_{IL}	Input Leakage Current		–400	µA	V_{IN} = 0.4 V, Notes 3, 4

NOTES:
1. This parameter is for inputs/outputs without an internal pull-up or pull-down.
2. This parameter is for inputs with an internal pull-down.
3. This parameter is for inputs with an internal pull-up.
4. This specification applies to the HITM# pin when it is driven as an input (e.g., in JTAG mode).

9.4 AC Specifications

The AC specifications consist of output delays, input setup requirements and input hold requirements. All AC specifications (with the exception of those for the TAP signals and APIC signals) are relative to the rising edge of the CLK input.

All timings are referenced to 1.5 volts for both “0” and “1” logic levels unless otherwise specified. Within the sampling window, a synchronous input must be stable for correct Pentium processor with MMX technology operation.

Each valid delay is specified for a 0 pF load. The system designer should use I/O buffer modeling to account for signal flight time delays.

Each Pentium processor with MMX technology specified to operate within a single bus-to-core ratio and a specific minimum to maximum bus frequency range (corresponding to a minimum to maximum core frequency range). Operation in other bus-to-core ratios or outside the specified operating frequency range is not supported. For example, the 166 MHz Pentium processor with MMX technology does not operate beyond the 66 MHz bus frequency and only supports the 2/5 bus-to-core ratio; it does not support the 1/3, 1/2, or 2/3 bus-to-core ratios. Table 50 summarizes these specifications.

Table 65. AC Specifications (Sheet 1 of 4)

See Table 61 for V_{CC} and T_{CASE} specifications, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	33.33	66.6	MHz	36	
t_{1a}	CLK Period	15.0	30.0	ns	36	
t_{1b}	CLK Period Stability		±250	ps		Adjacent Clocks, Notes 1, 25
t_2	CLK High Time	4.0		ns	36	2 V, Note 1
t_3	CLK Low Time	4.0		ns	36	0.8 V, Note 1
t_4	CLK Fall Time	0.15	1.5	ns	36	2.0 V – 0.8 V Notes 1, 5
t_5	CLK Rise Time	0.15	1.5	ns	36	0.8 V – 2.0 V Notes 1, 5
t_{6A}	PWT, PCD, CACHE# Valid Delay	1.0	7.0	ns	37	
t_{6b}	AP Valid Delay	1.0	8.5	ns	37	
t_{6c}	BE7#–BE0#, LOCK# Valid Delay	0.9	7.0	ns	37	4
t_{6d}	ADS# Valid Delay	0.8	6.0	ns	37	
t_{6e}	ADSC#, D/C#, W/R#, SCYC, Valid Delay	0.8	7.0	ns	37	
t_{6f}	M/IO# Valid Delay	0.8	5.9	ns	37	
t_{6g}	A16–A3 Valid Delay	0.5	6.6	ns	37	
t_{6h}	A31–A17 Valid Delay	0.6	6.6	ns	37	
t_7	ADS#, ADSC#, AP, A31–A3, PWT, PCD, BE7#–BE0#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	ns	38	1
t_{8a}	APCHK#, IERR#, FERR# Valid Delay	1.0	8.3	ns	37	4
t_{8b}	PCHK# Valid Delay	1.0	7.0	ns	37	4
t_{9a}	BREQ Valid Delay	1.0	8.0	ns	37	4
t_{9b}	SMIACT# Valid Delay	1.0	7.3	ns	37	4
t_{9c}	HLDA Valid Delay	1.0	6.8	ns	37	
t_{10a}	HIT# Valid Delay	1.0	6.8	ns	37	
t_{10b}	HITM# Valid Delay	0.7	6.0	ns	37	
t_{11a}	PM1–PM0, BP3–BP0 Valid Delay	1.0	10.0	ns	37	
t_{11b}	PRDY Valid Delay	1.0	8.0	ns	37	
t_{12}	D63–D0, DP7–DP0 Write Data Valid Delay	1.3	7.5	ns	37	
t_{13}	D63–D0, DP3–DP0 Write Data Float Delay		10.0	ns	38	1
t_{14}	A31–A5 Setup Time	6.0		ns	39	26
t_{15}	A31–A5 Hold Time	1.0		ns	39	
t_{16a}	INV, AP Setup Time	5.0		ns	39	
t_{16b}	EADS# Setup Time	5.0		ns	39	
t_{17}	EADS#, INV, AP Hold Time	1.0		ns	39	

NOTE: See Table 66 for notes.

Table 65. AC Specifications (Sheet 2 of 4)

See Table 61 for V_{CC} and T_{CASE} specifications, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{18a}	KEN# Setup Time	5.0		ns	39	
t_{18b}	NA#, WB/WT# Setup Time	4.5		ns	39	
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.0		ns	39	
t_{20}	BRDY#, BRDYC# Setup Time	5.0		ns	39	
t_{21}	BRDY#, BRDYC# Hold Time	1.0		ns	39	
t_{22}	AHOLD, BOFF# Setup Time	5.5		ns	39	
t_{23}	AHOLD, BOFF# Hold Time	1.0		ns	39	
t_{24a}	BUSCHK#, EWBE#, HOLD Setup Time	5.0		ns	39	
t_{24b}	PEN# Setup Time	4.8		ns	39	
t_{25a}	BUSCHK#, EWBE#, PEN# Hold Time	1.0		ns	39	
t_{25b}	HOLD Hold Time	1.5		ns	39	
t_{26}	A20M#, INTR, STPCLK# Setup Time	5.0		ns	39	Notes 12, 16
t_{27}	A20M#, INTR, STPCLK# Hold Time	1.0		ns	39	13
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.0		ns	39	Notes 12, 16, 17
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.0		ns	39	13
t_{30}	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2.0		CLK		Notes 15, 17
t_{31}	R/S# Setup Time	5.0		ns	39	Notes 12, 16, 17
t_{32}	R/S# Hold Time	1.0		ns	39	13
t_{33}	R/S# Pulse Width, Async.	2.0		CLK		Notes 15, 17
t_{34}	D0–D63, DP0–7 Read Data Setup Time	2.8		ns	39	
t_{35}	D0–D63, DP0–7 Read Data Hold Time	1.5		ns	39	
t_{36}	RESET Setup Time	5.0		ns	40	Notes 12, 16
t_{37}	RESET Hold Time	1.0		ns	40	13
t_{38}	RESET Pulse Width, V_{CC} & CLK Stable	15.0		CLK	40	17
t_{39}	RESET Active After V_{CC} & CLK Stable	1.0		ms	40	Power up
t_{40}	Reset Configuration Signals (INIT, FLUSH#) Setup Time	5.0		ns	40	Notes 12, 16, 17
t_{41}	Reset Configuration Signals (INIT, FLUSH#) Hold Time	1.0		ns	40	13
t_{42a}	Reset Configuration Signals (INIT, FLUSH#) Setup Time, Async.	2.0		CLK		To RESET falling edge, Note 16
t_{42b}	Reset Configuration Signals (INIT, FLUSH#, BRDYC#, BUSCHK#) Hold Time, Async.	2.0		CLK		To RESET falling edge, Note 27

NOTE: See Table 66 for notes.

Table 65. AC Specifications (Sheet 3 of 4)

See Table 61 for V_{CC} and T_{CASE} specifications, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{42c}	Reset Configuration Signals (BRDYC#, BUSCHK#) Setup Time, Async.	3.0		CLK		To RESET falling edge, Note 27
t_{43a}	BF0, BF1, CPUTYP Setup Time	1.0		ms	40	To RESET falling edge, Note 22
t_{43b}	BF0, BF1, CPUTYP Hold Time	2.0		CLK		To RESET falling edge, Note 22
t_{43c}	APICEN, BE4# Setup Time	2.0		CLK		To RESET falling edge
t_{43d}	APICEN, BE4# Hold Time	2.0		CLK		To RESET falling edge
t_{44}	TCK Frequency		16.0	MHz		
t_{45}	TCK Period	62.5		ns	36	
t_{46}	TCK High Time	25.0		ns	36	2 V, Note 1
t_{47}	TCK Low Time	25.0		ns	36	0.8 V Note 1
t_{48}	TCK Fall Time		5.0	ns	36	2.0 V – 0.8 V, Notes 1, 8, 9
t_{49}	TCK Rise Time		5.0	ns	36	0.8 V – 2.0 V, Notes 1, 8, 9
t_{50}	TRST# Pulse Width	40.0		ns	42	Asynchronous, Note 1
t_{51}	TDI, TMS Setup Time	5.0		ns	41	7
t_{52}	TDI, TMS Hold Time	13.0		ns	41	7
t_{53}	TDO Valid Delay	2.5	20.0	ns	41	8
t_{54}	TDO Float Delay		25.0	ns	41	Notes 1, 8
t_{55}	All Non-Test Outputs Valid Delay	2.5	20.0	ns	41	Notes 3, 8, 10
t_{56}	All Non-Test Outputs Float Delay		25.0	ns	41	Notes 1, 3, 8, 10
t_{57}	All Non-Test Inputs Setup Time	5.0		ns	41	Notes 3, 7, 10
t_{58}	All Non-Test Inputs Hold Time	13.0		ns	41	Notes 3, 7, 10
APIC AC Specifications						
t_{60a}	PICCLK Frequency	2.0	16.66	MHz	36	
t_{60b}	PICCLK Period	60.0	500.0	ns	36	
t_{60c}	PICCLK High Time	15.0		ns	36	
t_{60d}	PICCLK Low Time	15.0		ns	36	
t_{60e}	PICCLK Rise Time	0.15	2.5	ns	36	
t_{60f}	PICCLK Fall Time	0.15	2.5	ns	36	
t_{60g}	PICD1–PICD0 Setup Time	3.0		ns	39	To PICCLK
t_{60h}	PICD1–PICD0 Hold Time	2.5		ns	39	To PICCLK
t_{60i}	PICD1–PICD0 Valid Delay (LtoH)	4.0	38.0	ns	37	From PICCLK, Note 28
t_{60j}	PICD1–PICD0 Valid Delay (HtoL)	4.0	22.0	ns	37	From PICCLK, Note 28
t_{80a}	PBREQ#, PBGNT#, PHIT# Flight Time	0.0	2.0	ns	37	Notes 11, 24

NOTE: See Table 66 for notes.

Table 65. AC Specifications (Sheet 4 of 4)

See Table 61 for V_{CC} and T_{CASE} specifications, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{80b}	PHITM# Flight Time	0.0	1.8	ns	37	Notes 11, 24
t_{83a}	A31–A5 Setup Time	3.7		ns	39	18
t_{83b}	D/C#, W/R#, CACHE#, LOCK#, SCYC Setup Time	4.0		ns	39	Notes 18, 21
t_{83c}	ADS#, M/IO# Setup Time	5.8		ns	39	Notes 18, 21
t_{83d}	HIT#, HITM# Setup Time	6.0		ns	39	Notes 18, 21
t_{83e}	HLDA Setup Time	6.0		ns	39	Notes 18, 21
t_{84a}	CACHE#, HIT# Hold Time	1.0		ns	39	Notes 18, 21
t_{84b}	ADS#, D/C#, W/R#, M/IO#, A31–A5, HLDA, SCYC Hold Time	0.8		ns	39	Notes 18, 21
t_{84c}	LOCK# Hold Time	0.9		ns	39	Notes 18, 21
t_{84d}	HITM# Hold Time	0.7		ns	39	Notes 18, 21
t_{85}	DPEN# Valid Time		10.0	CLK		Notes 18, 19, 23
t_{86}	DPEN# Hold Time	2.0		CLK		Notes 18, 20, 23
t_{87}	APIC ID (BE3#–BE0#) Setup Time	2.0		CLK	40	To falling Edge of RESET, Note 23
t_{88}	APIC ID (BE3#–BE0#) Hold Time	2.0		CLK	40	From Falling Edge of RESET, Note 23
t_{89}	D/P# Valid Delay	1.0	8.0	ns	37	Primary Processor Only

NOTE: See Table 66 for notes.

Table 66. Notes for Table 65

NOTES:

Notes 2, 6 and 14 are general and apply to all standard TTL signals used with the Pentium® processor family.

Each valid delay is specified for a 0 pF load. The system designer should use I/O buffer models to account for signal flight time delays.

1. Not 100% tested. Guaranteed by design/characterization.
2. TTL input test waveforms are assumed to be 0 to 3 V transitions with 1 V/ns rise and fall times.
3. Non-test outputs and inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO and TMS). These timings correspond to the response of these signals due to boundary scan operations.
4. APCHK#, FERR#, HLDA, IERR#, LOCK# and PCHK# are glitch-free outputs. Glitch-free signals monotonically transition without false transitions.
5. 0.8 V/ns ≤ CLK input rise/fall time ≤ 8 V/ns.
6. 0.3 V/ns ≤ input rise/fall time ≤ 5 V/ns.
7. Referenced to TCK rising edge.
8. Referenced to TCK falling edge.
9. 1 ns can be added to the maximum TCK rise and fall times for every 10 MHz of frequency below 33 MHz.
10. During debugging, do not use the boundary scan timings (t_{55} to t_{58}).
11. This is a flight time specification, that includes both flight time and clock skew. The flight time is the time from where the unloaded driver crosses 1.5 V (50% of min V_{CC}), to where the receiver crosses the 1.5 V level (50% of min V_{CC}). See Figure 43. The minimum flight time minus the clock skew must be greater than zero.
12. Setup time is required to guarantee recognition on a specific clock. Pentium® processor with MMX™ technology must meet this specification for dual processor operation for the FLUSH# and RESET signals.
13. Hold time is required to guarantee recognition on a specific clock. Pentium processor with MMX technology must meet this specification for dual processor operation for the FLUSH# and RESET signals.
14. All TTL timings are referenced from 1.5 V.
15. To guarantee proper asynchronous recognition, the signal must have been deasserted (inactive) for a minimum of two clocks before being returned active and must meet the minimum pulse width.
16. This input may be driven asynchronously. However, when operating two processors in dual processing mode, FLUSH# and RESET must be asserted synchronously to both processors.
17. When driven asynchronously, RESET, NMI, FLUSH#, R/S#, INIT and SMI# must be deasserted (inactive) for a minimum of two clocks before being returned active.
18. Timings are valid only when dual processor is present.
19. Maximum time DPEN# is valid from rising edge of RESET.
20. Minimum time DPEN# is valid after falling edge of RESET.
21. The D/C#, M/IO#, W/R#, CACHE# and A31–A5 signals are sampled only on the CLK that ADS# is active.
22. In order to override the internal defaults and guarantee that the BF1–BF0 inputs remain stable while RESET is active, these pins should be strapped directly to or through a pull-up/pull-down resistor to V_{CC3} or ground. Driving these pins with active logic is not recommended unless stability during RESET can be guaranteed. Similarly, CPUTYP should also be strapped directly to or through a pull-up/pull-down resistor to V_{CC3} or ground.
23. RESET is synchronous in dual processing mode. All signals which have a setup or hold time with respect to a falling or rising edge of RESET in UP mode, should be measured with respect to the first processor clock edge in which RESET is sampled either active or inactive in dual processing mode.
24. The PHIT# and PHITM# signals operate at the core frequency.
25. These signals are measured on the rising edge of adjacent CLKs at 1.5 V. To ensure a 1:1 relationship between the amplitude of the input jitter and the internal and external clocks, the jitter frequency spectrum should not have any power spectrum peaking between 500 kHz and 1/3 of the CLK operating frequency. The amount of jitter present must be accounted for as a component of CLK skew between devices. The internal clock generator requires a constant frequency CLK input to within ±250 ps. Therefore, the CLK input cannot be changed dynamically.
26. In dual processing mode, timing t_{14} is replaced by t_{83a}. Timing t_{14} is required for external snooping (e.g., address setup to the CLK in which EADS# is sampled active) in both uniprocessor and dual processor modes.
27. BRDYC# and BUSCHK# are used as reset configuration signals to select buffer size.
28. This assumes an external pull-up resistor to V_{CC} and a lumped capacitive load. The pull-up resistor must be between 300 Ω and 1 KΩ, the capacitance must be between 20 pF and 120 pF, and the RC product must be between 6 ns and 36 ns. VOL for PICD1–PICD0 is 0.55 V.

Figure 36. Clock Waveform

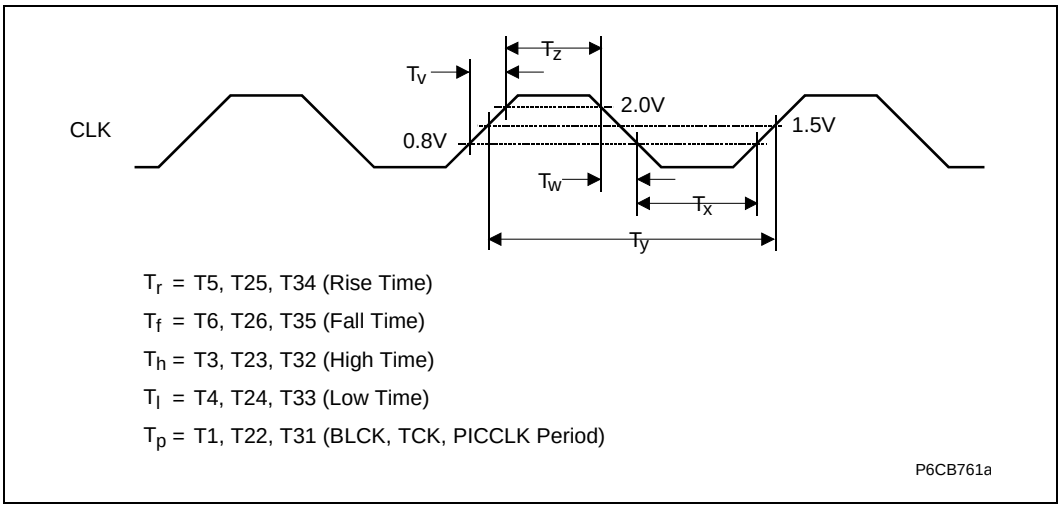

Figure 37. Valid Delay Timings

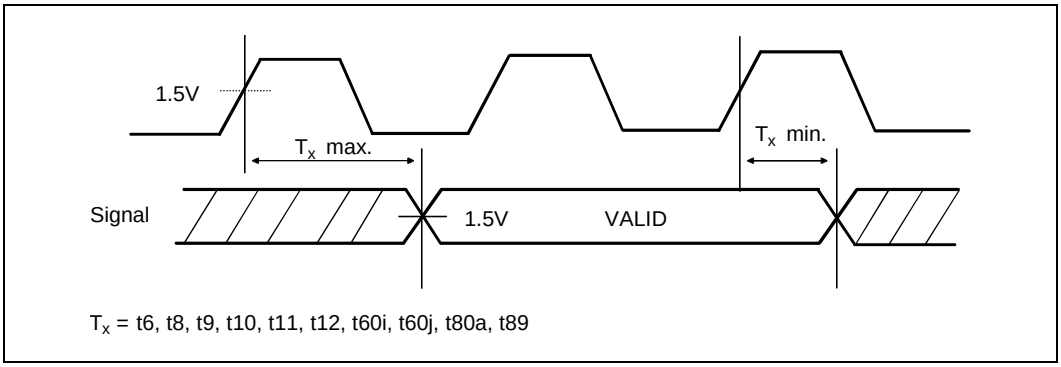

Figure 38. Float Delay Timings

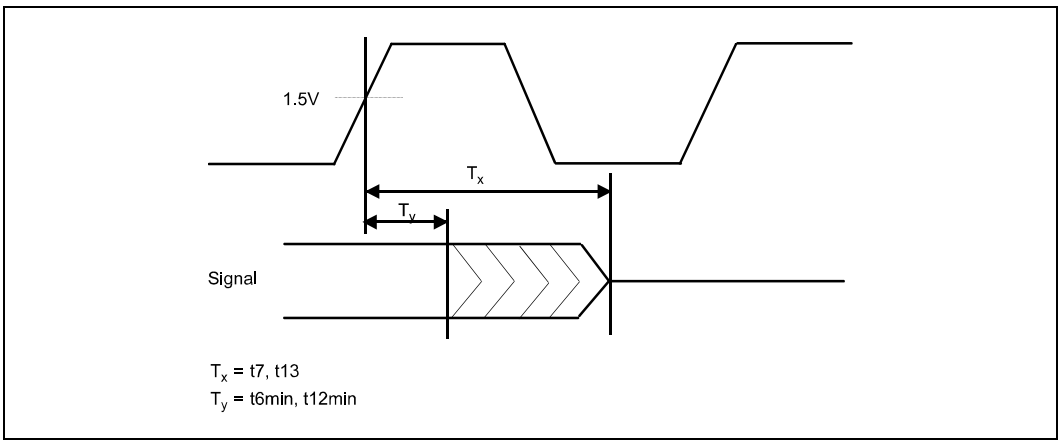

Figure 39. Setup and Hold Timings

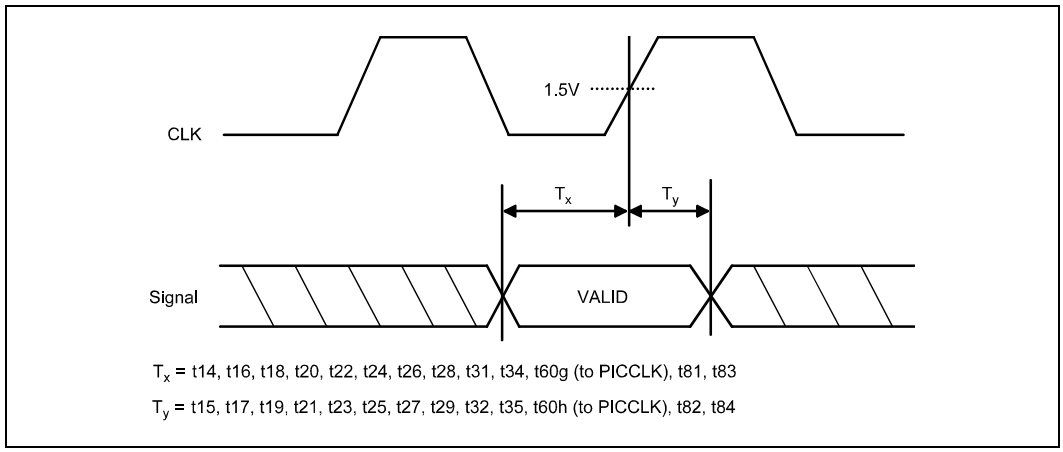

Figure 40. Reset and Configuration Timings

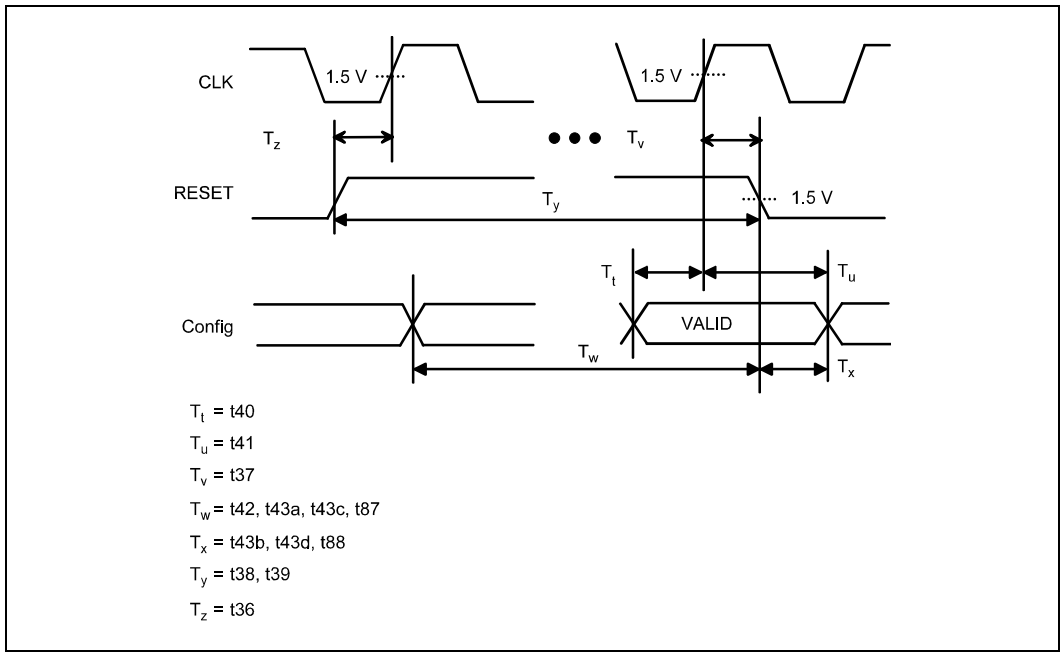

Figure 41. Test Timings

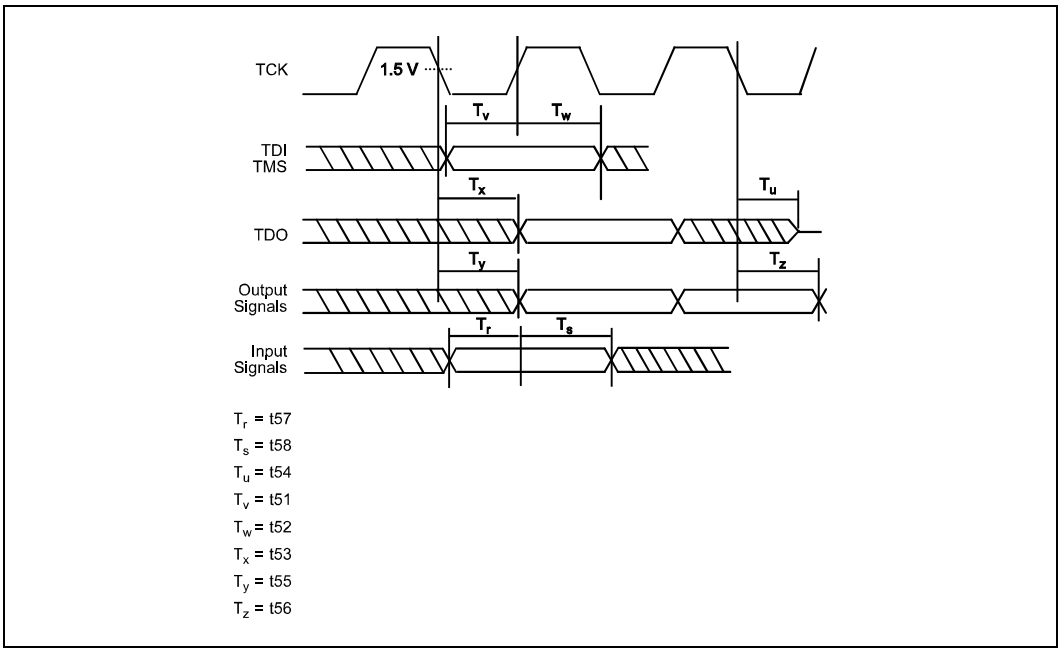

Figure 42. Test Reset Timings

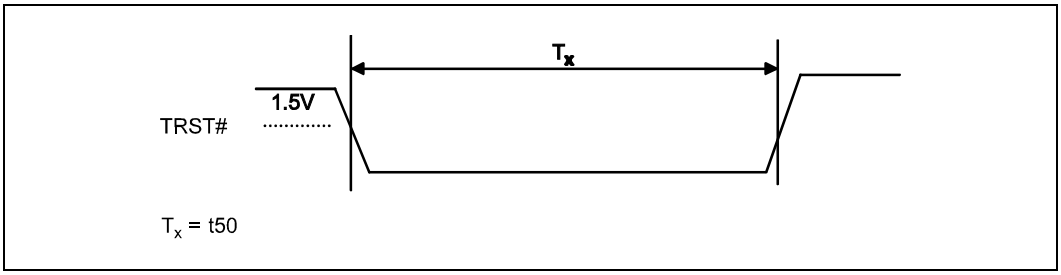

Figure 43. 50 Percent V_{CC} Measurement of Flight Time