System Management Mode in Am386 Microprocessors

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AMD's Am386DXLV™ and Am386SXLV™ microprocessors have a new operating mode called system management mode (SMM). SMM has a higher priority than the normal operating modes, and also provides the capability to implement I/O trapping. System designers can use this feature to control power to peripherals for power management. AMD's SMM is an optional feature; the system designer is free to use the processor without using SMM and implement traditional power-management techniques.

Programs running in this mode execute independently of the processor mode or operating system in a separate SMM memory space. This frees system and power management from dependence on the operating system. At the same time, it does not dictate features of the system solution because it allows flexibility and differentiation in the rest of the system logic. The system designer can design his own system logic to take advantage of SMM and I/O trapping, or choose from a myriad of chip-set vendors that support AMD's SMM.

Why SMM?

SMM is a hardware feature that eases the power-management software development effort, and provides the following benefits:

- SMM adds "user friendliness" to power management because a power-management menu for option control is available to the user in any operating system and environment.
- SMM reduces the complexity of power management for the user. Power management is always there, regardless of the operating system, with no drivers to install.
- I/O trapping enables power management of peripherals that are not "power aware."

The SMM consists of two features: a system-management interrupt (SMI) and I/O instruction break. SMM is implemented through a redefinition of four pins that are "no connect" pins on the standard 386DX and 386SX. The four new signals are SMI (system management interrupt), SMIADS and SMIRDY (handshake signals for the separate SMM memory space), and IIBEN (I/O instruction break enable).

System Management Interrupt

SMI is a non-maskable interrupt with higher priority than NMI and INTR. The execution of the SMI has four phases: interrupt initiation, processor state save, SMM code execution, and processor state restore and normal operation resumption.

A system management interrupt is initiated by driving the SMI pin active (low) or via software. Once the CPU recognizes the SMI, it will initiate a sequence to save the processor state in predetermined locations in the separate SMM memory space. The execution of SMM interrupt code then begins, fetching code from the SMM memory space. The SMM code can be executed in real or protected mode with an available address space of 4 Gbytes.

During the SMM code execution, I/O cycles, as a result of IN, OUT, and OUTS instructions, will go to the normal address space. This facilitates power-management code manipulating system hardware registers as needed through the standard I/O subsystem; a separate I/O space does not need to be implemented.

Returning to normal code execution in the main system memory, including restoring the processor state, is accomplished by executing a special code sequence. This code invokes a restore-CPU-state operation that reloads the CPU registers from the saved data in the RAM controlled by SMIADS and SMIRDY. After the completion of the restore state operation, normal code execution will continue at the point it left off before the SMI occurred.

When executing an SMM routine, the interrupt code can initiate memory data reads and writes to the main system memory using the normal ADS and READY pins. This is accomplished by using special forms of the MOV instruction.

The I/O instruction break feature is enabled by driving the IIBEN pin active (low). On detecting an I/O instruction, the processor will pause the execution unit, looking for SMI or READY. On sensing an I/O instruction to a peripheral device that needs power management (if it is powered off), the system logic can assert SMI. The SMM service routine can access the peripheral for which SMI was asserted and modify its state. Following the SMM routine, the I/O instruction that caused the break can be re-executed.

Conclusion

The core features of the system management modes offered by all manufacturers of 386 processors are basically the same. All include a hardware interrupt feature that invokes a mode-independent software routine in a

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with a system management mode.

SuperState V offers both hardware and software control. It traps on more conditions than Intel's or AMD's SMM, and SuperState V has no limit on the number of I/O addresses on which it can trap. SuperState can trap on hardware interrupts, software exceptions and interrupts, shutdown, and halt. The event capture ranges are specified through software parameters, rather than hardware signals, and while in the SuperState mode, access to normal user-mode memory is accomplished by using the simple GS prefix.

I/O events are faulted before execution rather than trapped afterwards, so there is no instruction retry and no complicated unwinding of the instruction stream, as required by Intel's SMM. A SuperState programmer simply powers up the device accessed by the trapped instruction and executes the faulted I/O instruction. Likewise, the system designer does not have to generate complicated signal sequences for each device that is powered-down to trap on I/O accesses to that device.

SuperState V provides several software features not found in Intel's or AMD's SMM. The new SCALL instruction allows privileged software to communicate with SuperState V code. The SuperVisor manages installation of multiple SuperState V applications and manages events. The SuperVisor's simple but robust programming interface (SPI) frees the programmer to simply use the SPI calls to manage events and resources, rather than coding from scratch. The SuperState V software advantage means faster development, greater functionality, and fewer problems. ♦

AMD SMM

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separate address space. Power management is the obvious application. Other functions that system management modes support include network drivers, device drivers, file translation software, data security, and supervision.

AMD's system management solution provides the core functions while leaving room for flexibility and differentiation for the system designer. This allows the designer to choose the chip set that best fits the requirements. Thus, the system architecture, chip count, and power-management approaches are selected by the designer, rather than dictated by the silicon supplier, as is the case with the Intel approach. This flexibility is extended to the I/O trapping feature in the solution offered by AMD, as multiple event ranges can be implemented. This approach is superior to the one offered by CHIPS and Technologies which has fixed internal event ranges for I/O trapping. ♦

Intel SMM

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The 82360SL peripheral unit contains the PC peripherals and most of the power-management resources. There are times when the latency of the SMI could corrupt the system integrity. In these cases, hardware is required to transparently delay the SMI until the time-critical event has completed. The 82360SL can generate an SMI interrupt from seven types of sources. The power-management resources are set up and controlled through many protected and visible I/O registers. The mapping and control of these power-management registers is now fixed, and all future SL products will have compatible mechanisms.

SMM Advantages

The i386 SL CPU is the lowest-risk solution for the newest generation of notebook computers, providing faster time-to-market for vendors and more robust, feature-rich systems for the end user. There are full-feature BIOS programs, controlling the Intel SMM power management, available from all the leading BIOS vendors. In addition, Intel provides a full-function in-circuit emulator, evaluation boards, and sample power-management code. The i386 SL microprocessor has been in production for the last year, and there are many proven notebook products already on the market. Intel is committed to future SL products and is currently developing the next generation. Only Intel provides the complete system solution by providing not only a special processor mode, but also a supporting peripheral chip, firmware, and development tools. ♦