Most Significant Bits

AMD Announces 486 Plans

As expected, AMD announced its plans to enter the 486 market later this year. Samples are promised for sometime this summer, with production in the fourth quarter; no pricing specifics were provided. The Am486DX will be offered in 25-, 33-, and 50-MHz speed grades, and the Am486SX will be provided only in a 25-MHz version; AMD will not offer the slower 16- and 20-MHz versions Intel has been selling.

AMD said that the 486 was being designed using the same methods used for the Am386. This implies that the chip will mimic Intel's logic design, with circuit-design changes to provide static operation and to allow use of a 3.3-V power supply. AMD said the 3.3-V parts, the Am486SXLV and Am486DXLV, will sample about three months after the 5-V version. The Am486 will be available in a plastic package, something that Intel has not yet offered. Intel has defined a plastic package for the 486SX but has not yet shipped it in that package.

AMD CEO Jerry Sanders would not discuss any further specifics of the Am486 design, saying that he didn't want to telegraph to Intel any more information than necessary. He specifically declined to say whether AMD would offer clock-doubler versions or larger cache sizes, saying only that there were no technical barriers to such enhancements and that AMD would offer what its customers wanted.

Enhancements such as a larger cache size could be important for convincing customers to use AMD's parts. In the 386 market, the majority AMD's business has come from the speed grades Intel did not offer: the 25-MHz 386SX and the 40-MHz 386DX. With the 486, Intel has been much more aggressive in pushing the clock rate, and Intel will not give AMD the opportunity to differentiate its 486 in this way. Features such as 3.3-V operation, static design, and plastic packaging will be important for portable computers, but they have little direct benefit in desktop designs and Intel will offer these features (with the possible exception of fully static design) as well.

With the 486, AMD is likely to compete more aggressively on price than it has with the 386, where it has been able to differentiate based on clock rate. As one indication of this strategy, Sanders said that AMD would price its 486DX-25 in plastic at only 20% more than the 486SX-25. Intel's current pricing (in thousands) is $319 for the 25-MHz 486SX and $417 for the 25-MHz 486DX—a 30% premium for the DX part. Since AMD will not offer the slower speed grades of the 486SX, however, it is likely to price its 25-MHz 486SX close to Intel's 16-MHz price, which is currently $202. A 20% premium over this price would be $242, far below Intel's current 486DX pricing.

Intel CEO Andy Grove told a meeting of financial analysts that Intel will offer 30 variations of its 386 and 486 processors this year. While these mostly will be simple speed, package, and power-supply-voltage variants, it nevertheless indicates that Intel will not make it as easy for AMD to find differentiation in the future as it was with the 386. In the meantime, however, AMD has established its credibility as a 386-compatible microprocessor supplier and established numerous customer relationships, so it may not be necessary to have the same degree of differentiation to achieve some market penetration.

386 Battle Advances

AMD also announced immediate availability of its 40-MHz 386DX in plastic, priced at $114 in thousands. This represents a significant price cut, since only a few weeks ago AMD quoted $130 for the 25-MHz version and $152 for the 33-MHz version, both in plastic. In the second quarter, AMD will drop the 25-MHz 386DX price to $94, and the 33-MHz version will be priced identically to the 40-MHz part at $114. Intel's fastest 386 is the 33-MHz version, available only in a PGA, priced at $190—67% higher than AMD's 40-MHz plastic part. To gain attention, AMD announced the 40-MHz chip at the second-quarter price, however, and Intel will also slash its prices in the second quarter.

Intel and AMD both moved their top 386SX speed grade up a notch, with AMD announcing a 33-MHz version and Intel finally offering the 25-MHz version that AMD has been shipping for months. AMD is pricing the 33-MHz chip identically to the 20- and 25-MHz versions, at $76 in thousands, dropping to $69 in the second quarter. Intel is pricing its 25-MHz part the same as its 20-MHz version, at $82.50 in thousands. With its 33-MHz version, AMD maintains its leadership in both price and performance.

The importance of maintaining a clock-rate lead—and the intensity of the competition between Intel and AMD—was illustrated by Compaq's recent introduction of a 25-MHz 386SX system. Sanders said that AMD had worked with Compaq on the design of that system and that he had a handshake agreement with now-departed Compaq CEO Rod Canion to use AMD's chips. At the last minute, however, Intel agreed to provide the 386SX at 25-MHz and Compaq decided to buy the chips from Intel. Sanders was clearly angered by the loss of Compaq's business, borrowing George Bush's line "this will not stand."

AMD's 386SX-33 gives the company an on-going advantage over Intel in high-volume, entry-level systems.

With no price premium for the 33-MHz version, the market is likely to move quickly to this clock rate. Two chip-set vendors, Oak Technology and ACC Micro, immediately announced 33-MHz versions of their 386SX system logic chips, and others are likely to follow.

Since the chip-set designs are very similar for SX and DX systems, they have already been tuned to run at 33 MHz and higher for the DX market, and offering the SX version at 33 MHz should be easy for most vendors.

Intel Counters with SL

Intel hopes to counter AMD's threat to its portable processor business by emphasizing the advantages of its 25-MHz 386SL. AMD's 33-MHz 386SX will put the SL at a performance disadvantage, however, putting pressure on Intel to move the SL up to 33 MHz.

Intel has not yet announced a 33-MHz 386SL, but it did recently introduce a lower-cost version. The new version, available only at 20 MHz, is simply a 386SL without the cache controller, and is priced at $101 in thousands—$25 less than the full-featured version at the same clock rate. It is fabricated from the same silicon as the standard part, which has on-chip cache tags as well as a cache controller, but these portions of the chip are not tested. Because the cache tags are a significant part of the chip area, Intel will be able to improve its yield and use otherwise defective chips by offering the cache-less version.

The cache-less 386SL will add a little more confusion to the notebook computer market, as buyers try to keep straight the differences between 386SX, 386SL, and cache-less 386SL, in addition to the range of clock rates. System makers using the cache-less version are unlikely to emphasize that fact, and system buyers accustomed to assuming a 386SL system has a cache will have to pay close attention to product specifications. At 20 MHz, however, the cache probably provides little benefit, so the performance difference might not be significant. The cache does reduce system power consumption, however, by reducing DRAM accesses, so cache-less 20-MHz systems may have a slightly shorter battery life than cached systems.

Intel also provided a glimpse of its SL roadmap, which includes a 3.3-V version of the 386SL in the first half of this year and a new chip, code named the H4C and likely to be called the 486SL, in the second half of the year. The H4C will be based on the 486 processor but will include additional on-chip features, including SMM support, and will operate at 3.3 V.

Intel and Microsoft Release APM Spec

The primary reason for the development of system-management modes in 386-architecture microprocessors was to enable power-management to be implemented in a manner that is independent of system software. (See pp. 16–19 for a comparison of the system-management modes offered by Intel, AMD, and C&T.) This approach has one weakness, however: the hardware often can't tell when the system is idle. Activity-detection hardware can shut down peripherals if they haven't been accessed for some period of time, but it is difficult to know when to slow down the processor. If a spreadsheet is recalculating, for example, there will be no I/O activity, but the user would like the processor to stay at full speed. No simple hardware mechanism can tell the difference between a system that is idle (but repeatedly executing its idle loop) and a system that is busy performing a long calculation.

The Advanced Power Management (APM) specification is designed to solve this problem by providing BIOS calls that allow application and operating-system software to tell the power-management firmware when the system is idle. The new calls include CPU Idle, CPU Busy, and Set Power State, plus ten other calls that provide other coordination functions. Microsoft has shipped an APM driver for DOS 5, and a driver for Windows 3.1 is promised "soon." The APM driver passes power-management information from applications to the BIOS, arbitrating among calls from multiple applications in a multitasking environment. It also generates APM calls on its own.

The APM interface requires an operating-system-specific driver. It does not negate the advantages of system management modes, however, because this driver is hardware-independent. By providing a standard interface, the APM calls enable the OS developer, instead of the hardware developer, to provide the OS-specific aspects of power-management software. Although the APM specification was codeveloped with Intel, it does not require any facilities unique to the 386SL and will be supported by AMD and C&T as well.

Copies of the APM specification are available from Intel sales offices and from Microsoft (206/882-8080).

GEC Plessey Licenses ARM Processors

GEC Plessey Semiconductors has signed a license with Advanced RISC Machines Ltd. to manufacture and sell the ARM processors and related devices, which until now have been available only from VLSI Technology. The agreement covers the existing ARM2, ARM3, and ARM600, as well as future ARM processors. GEC Plessey also has rights to incorporate the ARM processor cores in its own products. It plans to produce application-specific standard parts with on-chip analog and digital I/O functions, and it will also offer this capability to its ASIC customers.

Erratum

On page 4 of our 1/22/92 issue, the item about ULSI's math coprocessors mistakenly refers to IIT in two places. All company references in the item about ULSI should be to ULSI, not IIT. ♦