

## Resources

### Comcon to Feature New RISCs

In a striking break with tradition, this year's Comcon conference includes a number of significant presentations on new microprocessors. HP will present a paper on a superscalar PA-RISC implementation, as well as numerous talks on PA-RISC system design issues. Cypress/ROSS will describe, for the first time, its Pinnacle SPARC processor, and TI and Sun will describe the SuperSPARC processor and its companion cache controller. Motorola will present a session on its 88110 processor, including details of the graphics unit. DEC will describe its Alpha architecture and a single-chip VAX implementation.

Other sessions will cover embedded processors, multimedia technology and applications, transaction processing, mobile computing, network technology, cross-platform porting, and system architectures.

Eight tutorials will also be offered, including Yale Patt's traditional "Computer Architecture Choices," subtitled "What's New? and Why Bother?" Bus guru Paul Borrill, now at Sun, will present a tutorial on "Advances in Bus Architecture and Technology."

On a more entertaining note, Chuck Clanton will lead a tutorial on "Film Craft in User Interface Design," and in the session "The Silicon Behind the Silver Screen," Brian Kelly of LucasArts will discuss digital post-production issues and Lincoln Hu of ILM will discuss the computer-generated effects in *Terminator 2*.

The conference will be held on February 25-27 at the Cathedral Hill Hotel in San Francisco, with tutorials on the 24th and the 28th. To register or request more information, call 510/423-3490, fax to 510/423-9388, or send email to [comcon92@lbl.gov](mailto:comcon92@lbl.gov). Conference and tutorial registration are each \$300 for IEEE members, \$375 for others.

### RISC '92

Sponsored by Computer Design magazine, the RISC '92 conference program is being presented in conjunction with the Syscomp '92/West trade show, February 18-20. The show will be at the San Jose Convention Center, but the RISC '92 conference will be at the Le Baron Hotel. The conference program includes six half-day tutorials, covering the SPARC architecture; Intel's 860 and 960; the MIPS R3000/R4000; AMD's 29000; Motorola's 88110; and IBM's RS/6000. The program also includes several dozen one-hour lectures covering a variety of RISC processors and system design issues.

Registration covers all three days of tutorials and lectures, and costs \$495 in advance (\$545 at the door). Call 800/458-0011 to register, or send a fax to 508/692-7780.

### IEEE Multichip Module Conference

This conference will feature a wide variety of talks on multichip module technology and applications, including a keynote address by John Hennessy on "The Impact of MCM Technology on Computer Architectures." Other microprocessor-related talks include "Design of a Silicon-on-Silicon Multichip Module for a High-Performance PS/2 Workstation," to be presented by IBM, and a talk from Silicon Graphics on a "Multichip R3000/R3010 Module."

Conference registration (if sent by March 1) is \$235 for IEEE members, \$300 for others. The conference will be held on March 18-20 at the Cocomat Grove in Santa Cruz, CA. Four half-day tutorials will be held on March 17; the tutorial fee is \$50 each for IEEE members, \$75 each for others. For information, contact Jean McKnight, Computer Engineering, UCSC, Santa Cruz, CA 95064; 408/459-2303; email [jean@cse.ucsc.edu](mailto:jean@cse.ucsc.edu).

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