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DEC Enters Microprocessor Business with Alpha

DEC to Sell Chips on Open Market

By Brian Case and Michael Slater

Digital Equipment Corp. has jumped into the microprocessor business with the fastest chip yet announced, offering its Alpha microprocessor for sale on the merchant market. DEC will use Alpha in workstations and multiuser systems, and it will market it at the architecture, chip, board, and system levels.

At a 200-MHz clock rate, DEC expects the chip to perform at over 150 SPECmarks. DEC promises that it will ship systems at this clock rate, although the initial merchant-market chip, called the 21064-AA, will be specified for "only" 150-MHz operation. DEC claims that the mid-point of its yield distribution is 170 MHz. Extrapolating from the 200-MHz SPECmark claim, the 150-MHz device should perform at over 110 SPECmarks. No specific benchmark data has been released.

DEC is seeking semiconductor companies to manufacture the chip as an alternate source to DEC's own fab. Since DEC will offer the chips directly, however, chips will be available on the open market regardless of DEC's success in signing up semiconductor licensees.

The only major U.S. semiconductor company that has not licensed a RISC architecture is National Semiconductor, and National is rumored to be in discussions with DEC. Other prospects include SGS-Thomson, whose transputer hasn't made any inroads in the workstation market; a few major Japanese companies that haven't yet signed up for a RISC architecture, such as Sanyo and Sharp; and companies that have licensed one of the other RISC architectures but are willing to take on a second one.

For software support, DEC will offer at least two operating systems: VMS (the VAX operating system) and its implementation of OSF/1 UNIX. DEC is promising source-level compatibility between Alpha, MIPS, and Intel x86 versions of OSF/1, and between Alpha and VAX versions of VMS. Both OSF/1 and VMS on Alpha are promised to ship by the end of this year. The OSF/1 implementation will support 64-bit addressing, but for software compatibility reasons, VMS will not.

DEC has developed binary porting tools that make it possible to move either MIPS or VAX code to the Alpha environment without recompilation. The performance degradation is highly dependent on the application, and DEC views the binary porting tools as a short-term bridge, not as a long-term alternative to recompilation.

DEC is negotiating with Microsoft for a Windows NT port to Alpha, and Bill Gates confirmed in a Wall Street Journal interview that Microsoft will work with DEC. Microsoft has its hands full getting the x86 and MIPS ports out the door, so it seems surprising that it would be willing to take on another RISC port—especially to an architecture with no installed base.

As part of the Alpha program, DEC has announced its embracing of "open business practices" that marks the culmination of a transition that began with its offer-

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DEC's Alpha

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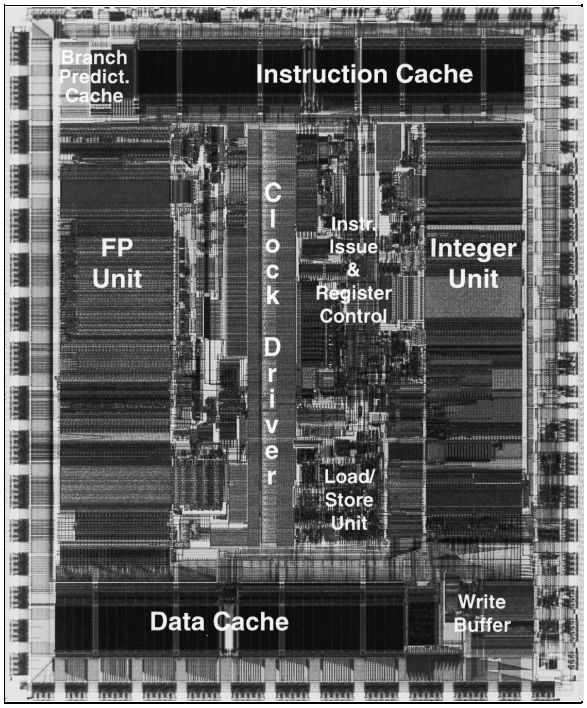
ing of MIPS-based workstations three years ago. In addition to offering Alpha chips, boards, and systems, DEC will also offer for licensing the VMS and OSF operating systems. This is, in a sense, the end of the proprietary VAX standard, although DEC will continue to produce VAX systems. Other companies will now be able to build Alpha VMS systems, to which many VAX users are likely to switch over the next few years.

DEC has two initial system makers signed up for Alpha: Cray Research, which plans to use it in massively parallel machines, and Kubota, which will build high-end graphics workstations, adding to its "Titan" line. Kubota says that it will continue to enhance its MIPS-based workstations as well, and will provide source-level compatibility and interoperability between the two product lines.

DEC has not detailed its system plans, other than to say that system products will be announced and shipped by the end of this year. The first systems are likely to be designed as VAX replacements, implying a large-system design and price. Workstations are also planned, but they will not initially reach the lower end of the MIPS-based workstation price spectrum.

Alpha is a discouraging development for MIPS, since it shows DEC is not committed to the MIPS architecture as a long-term strategy. Kubota is also a MIPS investor and licensee, and it appears that both companies have lost faith in MIPS' ability to keep them on the leading edge.



DEC's 21064 Alpha chip, which includes 1.68 million transistors on a 550 × 660 mil (13.9 × 16.8 mm) die.

Alpha Technology

The Alpha architecture is, in most respects, a traditional RISC design. It is unusual in that it is a 64-bit architecture, with no 32-bit subset defined, and it has been designed with more consideration for high-clock-rate, multiple-issue implementations than other architectures. (See p. 10 for details on the architecture.) While some architects disagree with a few of the architectural decisions, it seems clear that, from a purely technical viewpoint, it is superior to the existing RISC architectures—at least for high-end implementations.

DEC is, however, introducing Alpha into a market that is likely to be largely unreceptive. There are already a number of competing RISC architectures, and promises and rumors of advanced implementations of each are rampant. DEC is, at best, the fifth processor vendor to make the rounds of system and semiconductor companies seeking to license its architecture. SPARC and MIPS began this process several years ago, and in the past year or two HP and IBM have joined in as well. While Alpha may be a superior architecture, the architectural differences seem unlikely to be important enough to be significant for most applications.

It is to DEC's credit, then, that the first implementation of Alpha is of unprecedented technological strength. The 200 MHz operating frequency of the first Alpha chip—yielding a supercomputer-class 5 ns clock cycle—is at a level many thought could only be achieved with exotic technologies such as GaAs. It is especially impressive given that this is a two-issue, superscalar implementation. Until now, the fastest clock speed has been the R4000's internal rate of 100 MHz, but the R4000 is a single-issue design. Sun's BiCMOS SuperSPARC design is struggling to get to 50 MHz; IBM's multichip RS/6000 implementation has only recently reached 50 MHz, and the single-chip version is being shipped only at 33 MHz.

DEC says that any industry-standard sub-micron CMOS fabrication line has the equipment needed to run DEC's CMOS-4 process used for the 21064, but it will require significant changes to the process "recipe."

Some of Alpha's clock-speed advantage is due to the streamlining in the architecture. For example, the lack of support for 8- and 16-bit loads and stores eliminates a multiplexer from a critical timing path. The superscalar implementation is also eased by the lack of load and branch delay slots, the lack of condition codes, and the imprecise exception model.

Much of the clock-rate advantage, however, arises from DEC's design focus: it set out to build the fastest possible processor, without compromises to reduce chip cost or simplify system design. Examples of costs that DEC incurred to support the high clock rate are the large portion of the chip devoted to clock buffers and the very high power consumption—30 watts at 200 MHz.

While processor implementation has always been a

game of leap-frog, it seems unlikely that any other processor architecture will soon have an implementation that will beat this first Alpha implementation in raw clock speed. Application-level performance in mainstream desktop systems is another matter, however, and it is less clear that Alpha will maintain a lead in this regard (see editorial on p. 3).

DEC's RISC History

This is the third RISC architecture DEC has designed, but it is the first to reach the marketplace. The first was Titan, a research project started in 1984 at DEC's Western Research Laboratory and headed by Forest Baskett and Norm Jouppi. Titan was implemented in ECL, and DEC never committed to making it a commercial product.

The second RISC machine designed by DEC was Prism, created by a team led by Dave Cutler (who had previously led the development of VMS), starting in 1985. Just before the first Prism chips were fabricated, however, DEC management decided to adopt the MIPS architecture. The Prism chip was faster than the chips MIPS had at the time, but MIPS had a more advanced compiler suite and a body of applications. DEC was also beginning to make the transition to the open systems world, and adopting an open, standard architecture was a natural way to do this. There was considerable dissension within DEC about the decision to drop Prism, and Dave Cutler left the company in protest. He now heads the Windows NT development team at Microsoft, where, ironically, he is leading the port of Windows NT to the MIPS architecture.

The Alpha project began in mid-1989 to provide a migration path for VAX customers. DEC recognized that it would not be able to keep the VAX architecture performance-competitive, so the decision was made to develop a new architecture to which the VMS operating system could be ported. At that time, DEC planned to stick with the MIPS architecture for its UNIX offerings.

As the Alpha project progressed, however, it became clear that it would significantly out-perform the MIPS products. This is due, in part, to disappointing results from the MIPS ECL project, which DEC originally viewed as critical but later decided not to pursue. The R4000 also came to market later than hoped and with a lower performance level than DEC expected.

As a result, DEC now appears to have focused the future of the company on the Alpha architecture. It will continue to develop and market MIPS-based systems as well as VAX systems, but it is clear from DEC's posturing that it expects to gradually move all its customers to Alpha-based products.

Implementation Overview

The first Alpha implementation is a large, 550×660 mil (13.9×16.8 mm) CMOS chip with 1.68 million transistors. The CMOS process is described as a 0.75 micron, 3-layer metal technology, with a 0.5-micron channel length. The top layer of metal in this process is especially thick so it can carry the large currents required, and to increase the reliability of the clock distribution network.

The transistor count is low for such a large die, at least by the standards of SuperSPARC, but Alpha implements less cache and a full, 64-bit integer data path, factors that lower the raw transistor count. Also, significant area is spent accommodating the high frequency of operation and the high power impulses that result from switching transistors at such a high clock rate. The peak internal current during clock switching is a staggering 43 amps.

The chip dissipates an awe-inspiring 30 watts at 200 MHz with a 3.3-V power supply; it draws an incredible 9 amps average supply current. At 150 MHz, power dissipation is 23 W typical and 27.5 W maximum. About half the current is dissipated in the clock-generation and distribution circuitry. To dissipate the generated heat, the 431-pin through-hole PGA package includes two threaded slugs to which a large, finned heat sink is bolted. No doubt the large number of pins helps dissipate some heat as well, but the pins probably also create a few PC-board routing problems.

The extremely high frequency of operation is achieved through a combination of techniques. First, a low-voltage, 3.3-V CMOS technology reduces signal swing. Custom circuit design techniques are used throughout, and very little logic is designed with synthesis tools. This implementation shows that a hand-optimized, full-custom design can yield results unobtainable with automatic design tools.

Where necessary, brute force is used in the design. For example, a 128 nF on-chip decoupling capacitor is used to buffer current spikes that would otherwise compromise signal integrity. To minimize clock skew, gargantuan 250K-micron transistors are used in the clock

Price & Availability

Evaluation samples of the initial Alpha microprocessor, officially called the 21064-AA, are available now. Volume shipments are scheduled to begin in July. Pricing is $3375 for samples; $1650 for more than 100 units; and $1559 in quantities of over 1000.

The Alpha Architecture Handbook is available now, along with a brief summary of the 21064's specifications. As of press time, a full data sheet has not been released; DEC expects to have it available in about four weeks. Contact your local DEC sales office, or call 800/DEC-2717 or 508/568-6868.

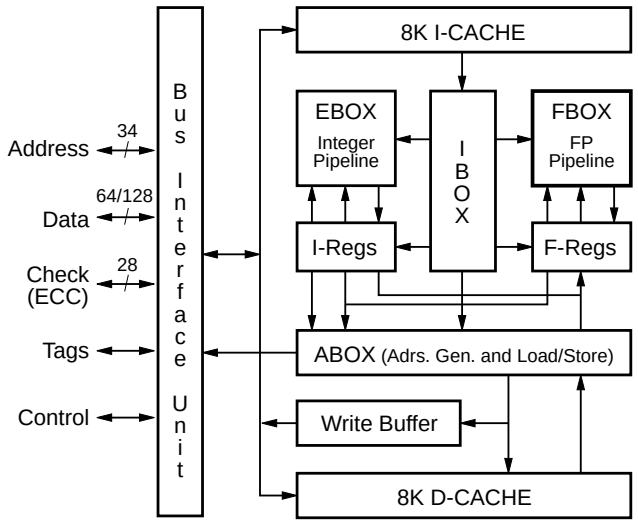


Figure 1. Block diagram of the Alpha chip.

driver. Extensive analysis of clock distribution was necessary to insure minimum skew. The chip requires a 2× clock input—400 MHz for 200-MHz operation.

The bus interface can be either TTL-compatible or 100K ECL-compatible, as selected by a configuration pin at power-up. Even though the chip operates from a 3.3-V power supply, it interfaces directly to 5-V logic.

The external data bus can be configured to be either 64 or 128 bits wide, and the bus clock can be selected to be from one-half to one-eighth of the processor clock rate. Full ECC support is provided for the external bus. Writes are queued in an on-chip write buffer that can hold four lines of 32 bytes each.

The external address bus is 34 bits wide. Although the Alpha architecture has 64-bit linear virtual addresses, this chip implements "only" a 43-bit virtual address (the R4000, for comparison, implements a 40-bit virtual address in user mode).

The chip includes separate 8-Kbyte, direct-mapped, physically-addressed data and instruction caches with 32-byte lines and 32-byte refill sizes. The cache uses 6-transistor cells, and comprises about 900,000 transistors. Address translation is performed by two fully-associative TLBs. The data TLB has 32 entries, which can map pages of 8K, 64K, 256K, or 4M bytes. The instruction TLB has twelve entries, eight that map 8K pages and four that map 4M pages.

An external, second-level cache of 128K to 8M bytes can be implemented using standard SRAMs. The 21064 provides all the control logic necessary to handle the speed-critical case of a cache hit. An external state machine is required to implement the cache policy for handling cache misses, as well as snooping for cache coherency. Timing for the external cache can be programmed to be 3 to 16 processor cycles. A 3-cycle external cache would require 8-ns ECL RAMs at 200 MHz; typical high-end designs are likely to settle for a 4-cycle cache access, which allows 10-ns RAMs to be used.

Load/Store	+	Floating or Integer Operation
Integer Operation	+	Floating Operation
Floating Operation	+	Floating Branch
Integer Operation	+	Integer Branch
Except:		
Integer Store	+	Floating Operation
Floating Store	+	Integer Operation

Figure 2. Alpha issue capabilities.

To ease system debug, the 21064 loads its internal cache at reset via a serial link to a small EEPROM. This allows test routines to be executed without requiring that the main memory system be functional.

Superscalar Capabilities

The chip is superpipelined—like the MIPS R4000—to minimize cycle time, and it has a superscalar organization—similar to IBM's RS/6000—to maximize instruction throughput. Figure 1 shows a block diagram of the chip. The IBOX is responsible for instruction fetch and dispatch to the four independent function units. The EBOX is the integer ALU and pipeline. The FBOX is the floating-point adder, multiplier, and other FP pipeline stages. The ABOX is the address translation and load/store unit.

Figure 2 shows the instruction issue rules. The superscalar capabilities implied by these rules are much like those of IBM's multichip RS/6000 implementation of the POWER architecture. Under favorable circumstances, the RS/6000 implementation can issue three or even four instructions in a cycle, although such circumstances are probably rare. The 21064 can issue a maximum of two instructions in a cycle, but it can do so for most of the common instruction pairs.

Neither the RS/6000 nor the 21064 implementation goes beyond the natural parallelism suggested by the functional units present in all pipelined implementations (integer ALU, FP ALU, load/store unit, and branch unit). In particular, unlike Sun/TI's SuperSPARC and Motorola's 88110, neither machine can issue two integer operations in the same cycle. To do so in an Alpha processor would require two relatively expensive 64-bit integer data paths.

Pipelines

Figure 3 shows the integer pipeline of both the 21064 and the philosophically similar R4000. The arrows pointing to the left show the register file bypass paths. The same arguments made about whether or not the R4000 is superpipelined can be made about the 21064. As implied by the bypass paths, both implementations can complete an integer ALU operation in one

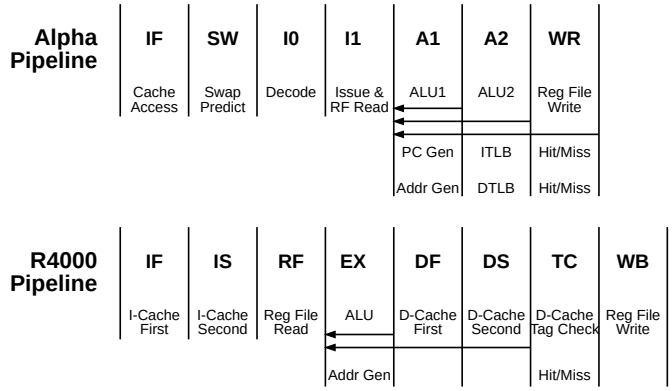


Figure 3. Comparing Alpha's integer pipeline with the R4000.

cycle. The key difference, of course, is that the R4000 issues only one instruction during each clock cycle, while the 21064 can issue two.

In the 21064 pipeline, integer arithmetic and logic operations are completed in the ALU1 stage and piped forward in ALU2. Thus, these operations have a single-cycle latency, and dependent operations can occur on successive cycles. Shift operations use both ALU and ALU2, so they have a two-cycle latency and back-to-back dependent shifts cause a one-cycle stall. The shifter is fully pipelined, so independent shifts can be issued every cycle.

For data cache accesses, a dedicated adder in the ABOX calculates the virtual address during ALU1. In ALU2, the address is translated by the TLB, and, in parallel, the cache is indexed. (Since the page size is the same as the cache size, the address bits used to index the cache are the same for virtual and physical addresses.) Data from the cache is written to the register file in the WR stage. Load latency is three cycles, just like for the R4000 (i.e., for no stall to occur, a load must be followed by at least two instructions that do not use the result of the load). The pipeline is fully interlocked.

The 21064 requires an additional stage of instruction decode, as compared to the R4000, to check for opportunities to issue two instructions in a cycle; the SW stage is used to direct instructions to the appropriate pipelines. Even though the 21064 pipeline is one stage shorter, its ALU stage is one clock later. This means that pipeline breaks, such as those caused by mis-predicted branches, cost an extra cycle for Alpha. Branch prediction is used to eliminate stalls on branches in most cases, but when the prediction fails, the branch penalty is 4 cycles.

Figure 4 shows the 21064 floating-point pipeline. As with the integer pipeline, the first four stages are associated with the IBOX instruction fetching and dispatching logic. The remainder of the FP pipeline is similar to the pipelines of other implementations.

All operations are fully pipelined (i.e., they can be

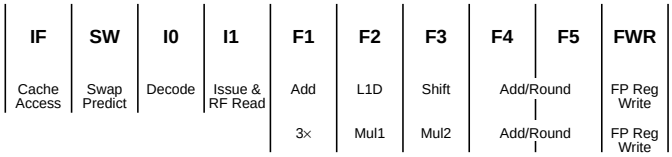


Figure 4. Alpha floating-point pipeline.

issued at a rate of one per cycle), except for integer multiply and floating-point divide (there is no integer divide). Integer multiply has a latency of 21 cycles for longwords (32 bits) and 23 cycles for quadwords (64 bits). Floating-point divide latency is 31 cycles for single-precision and 61 cycles for double-precision. Unrelated instructions are not blocked during execution of these long-latency instructions.

Conclusions

This first implementation of the Alpha architecture establishes a new high ground for microprocessor performance. It will certainly have an impact on the computer market, if only in high-end DEC machines running VMS. As a replacement for the VAX, the Alpha architecture and the initial implementation are clearly superb designs.

More important to DEC's competitors, even the initial Alpha implementation could be the basis for workstations of moderate cost. DEC is also developing both lower-cost and higher-performance implementations, which will broaden the threat to other architectures. An Alpha workstation could cause serious problems for HP and IBM, if not Sun. Many Sun customers are loyal because of the software base, but HP and IBM customers are probably more mobile. Just as HP and IBM have been able to capture significant fractions of the workstation market by leap-frogging the performance of SPARC and MIPS systems, Alpha-based workstations could take away some of HP's and IBM's market.

The continued dominance of Sun in the workstation market is testimony, however, to the fact that top performance is not the only thing that sells workstations. With its MIPS-based systems, DEC has been very competitive with Sun on price, performance, and price/performance, but Sun continues to out-ship DEC by a considerable margin. The reason, of course, is software—many workstation customers continue to buy SPARC-based systems because they are the only workstations that can run all the software they need. In time, this edge will lessen, but the fact that HP and IBM still suffer from a lack of software illustrates how long it takes to build a competitive software base.

The announcement of Alpha seems to put the future of DEC's MIPS-based line of workstations in imminent jeopardy. DEC categorically denies any immediate

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low-level hardware resources such as the processor status register and address-translation hardware.

Architecture Evaluation

One of the main goals of Alpha is to make sure that its implementations are as fast as technology will allow. This is nothing new, since RISC was invented to exploit hardware, but Alpha does indeed go a couple of steps beyond other RISCs in catering to fast implementations. The lack of byte and 16-bit loads and stores helps to minimize the logic between the processor and first-level cache and simplifies ECC and sequencing in write-back caches. Superscalar implementations should be easier to design because there are no delayed branches, no shared resources, and no precise exceptions. Condition codes (as in IBM POWER) and multiply-quotient registers (as in MIPS) are examples of shared resources that can complicate superscalar implementations.

Still, Alpha has its drawbacks. The tremendous overhead paid for loads and stores of small data is the most glaring. One of the golden rules of architecture and implementation is that anything that makes the basic instruction cycle faster is probably worthwhile. Nonetheless, the improvement in basic instruction timing allowed by eliminating byte and 16-bit loads and stores must be quite significant to overcome the cost of the long instruction sequences required. DEC says that fewer than 8% of VAX/VMS memory references deal with quantities smaller than 32 bits, and that many of these are string searches or copies that can be performed with longword or quadword accesses. For byte and word I/O operations, DEC's plan is to shift I/O addresses left four bits and use the four lower address bits as byte enables.

Alpha does indeed facilitate fast, superscalar implementations better than other RISCs, but it is still possible to design and build superscalar implementations of other RISCs in a reasonable amount of time and chip area. The original RISC characteristics (load/store architecture, three-address operations, single-sized instructions, simple formats, instructions that fit in a uniform pipeline, etc.) have a first-order effect on implementation and software quality. While the advantages of the Alpha architecture are real, they are of only second-order significance.

What is more important for DEC is the architectural support for misaligned data and VAX FP operands—features that are not found in other RISCs. DEC's motivations for creating a new architecture are best understood in light of its need to provide an efficient VAX replacement. For applications where VAX compatibility is not a concern, it does not appear that Alpha's advantages are great enough to overcome the advantages of the software base and momentum of existing architectures. ♦

Alpha Implementation

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plans to stop MIPS-based development—R4000 system development is said to be well underway—but they also point out that Alpha products will have to be competitive. This seems to imply that customers will have a choice of MIPS- and Alpha-based workstations in similar price ranges. DEC's aggressive promotion of Alpha could considerably weaken the marketability of DEC's MIPS-based workstations, despite assurances of a smooth migration path.

Despite Alpha's impressive performance and architectural edge, each of the leading RISC architectures has important advantages. SPARC and MIPS both have the advantage of a wide range of implementations now available or expected soon, and a similar range of implementations is promised for PowerPC. It remains to be seen how quickly DEC will be able to develop a range of implementations and how aggressively it will pursue the low end of the market, which is where the volume is.

For the MIPS architecture, in comparison, there are low-end chips such as IDT's R3081 and Performance Semiconductor's PIPER that will compete effectively with the 486; today's R4000, which is a good mid-range device; future R4000s with higher clock rates and larger caches; and future R4000s aimed at lower-cost systems.

PowerPC remains the only RISC architecture with a clear path to the personal productivity computer market, thanks to Apple's commitment to migrate its Macintosh line. MIPS may have the second-best chance because of Windows NT, but its ability to compete with the x86 remains in question. SPARC continues to do well in the technical workstation market because of its software edge, and Sun has begun penetrating some commercial applications where a wide variety of personal productivity software is not required. Alpha seems unlikely to blunt any of these advantages.

In the workstation arena, HP is likely to be the most threatened by Alpha. HP has taken a very slow, cautious approach to licensing its architecture, and it has been unwilling to take on the support burden of selling its chips on the merchant market. DEC's more aggressive approach could create considerable trouble for HP, which remains outside the mainstream. HP expects its latest implementation, the 7100, to run at 100 MHz with a performance level of 120 SPECmarks—about the same as the 21064 at 150 MHz.

From a business perspective, it seems a shame that DEC did not apply its chip design and fabrication capabilities to the MIPS architecture, perhaps with extensions to better support VAX software. That they did not do so is perhaps evidence of the difficulty a company such as DEC has with basing its business on an architecture from an outside supplier. ♦